'89.

GS MOS MEMORY DATA BOOK

- SRAM
- DRAM
- MASK ROM

ELECTRONIC MANUFACTURERS' AGENTS
309 Jordan Lane, N.W.
Huntsville, Alabama 35805
(205) 830-4030
(800) 633-2920

GoldStar
GOLDSTAR ELECTRON CO., LTD.

GS
MOS MEMORY
DATA BOOK

- SRAM
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GoldStar

GoldStar Semiconductor Group
MANUAL & DATA BOOK LIST

1) GS PRODUCT GUIDE
2) Z80 FAMILY DATA BOOK
3) GS TTL DATA BOOK
4) GS HIGH SPEED CMOS LOGIC DATA BOOK
5) MOS LOGIC GD4000 SERIES DATA BOOK
6) GS LINEAR DATA BOOK
7) GS MEMORY DATA BOOK
8) CMOS GATE ARRAY DATA BOOK
9) GMCS404C USER MANUAL

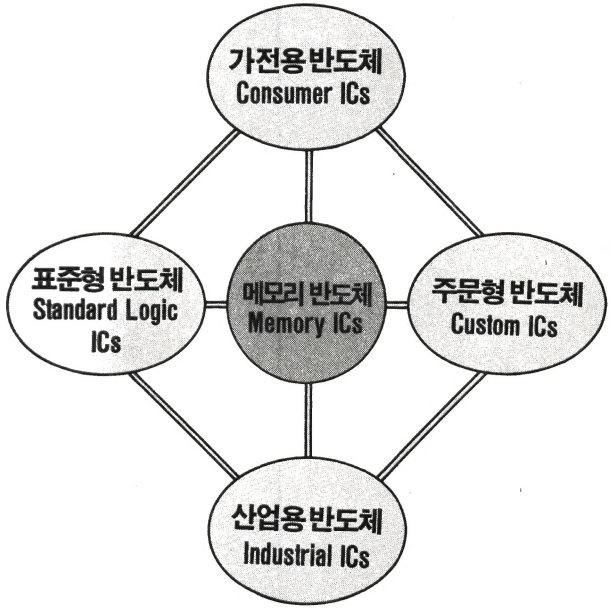
■ Product Status

DEFINITIONS		
Data Sheet Indentification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. GoldStar reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. GoldStar reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Preface

In this age of electronic information and communication systems, semiconductors have become an increasingly important component in the lives of people everywhere. Aware of the necessity for semiconductors that save time and conserve energy, GoldStar is committed to the development of ever more sophisticated innovations in this vital industry.

Modern industry makes use of semiconductors with a wide variety of functions in very phase of planning, production and distribution. GoldStar, ever mindful of its goal to become a leader in every one of its fields of endeavor, continues to diversify its activities and now produces semiconductors in each production line in the industry, including logic, memory, industrial, consumer and custom semiconductors.



According to the company's short-term strategy for maintaining its steady rate of growth, GoldStar focuses its considerable energies on standard and memory semiconductors.

Having succeeded in the development of such sophisticated products as the 256K SRAM, 1M DRAM, high-speed CMOS 256K DRAM, 1 chip color TV IC, and 2 chip VCR IC, GoldStar is now making progress in its research on up-to-the-minute technologies for the development of the 4M DRAM and GaAs compound semiconductors.

This 1989 GoldStar Memory DataBook contains data on currently available Memory products and some products which are planned for the immediate future.
We are continually developing and introducing new products of high quality, high performance and high reliability and we sincerely hope you will find this catalog for design engineers useful.

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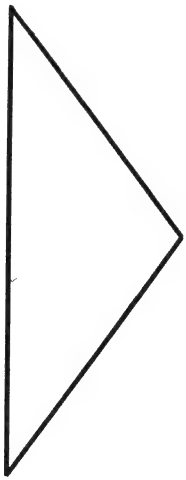


PRODUCT INDEX

RAMS

STATIC RAM

PROCESS	ORG	TYPE NO.	ACCESS TIME (MAX ns)	POWER ACTIVE	POWER S/B	FEATURE	PACKAGE (MIL)	AVAILABLE
CMOS	2K x 8	GM76C28 - 10	100 ns	60 mA	50 uA		24 DIP/(600)	NOW
		- 12	120	50 mA				
	8K x 8	GM76C88 - 85	85 ns	110 mA	2 mA		28 DIP/SOP (600/330)	NOW
		- 10	100					
		- 12	120					
		GM76C88L - 15	150 ns	40 mA	100 uA	L-POWER	28 DIP/SOP (600/330)	3Q/'89
		GM56C88 - 35	35 ns	100 mA	30 mA	H-SPEED	28 DIP (300)	3Q/'89
		45	45					
		55	55					
	16K x 4	GM56C164 - 25	25 ns	70 mA	30 mA	H-SPEED	22 DIP (300)	3Q/'89
		- 35	35					
		- 45	45					
	32K x 8	GM76C256/L - 85	85 ns	70 mA	1mA		28 DIP/SOP (600/330)	1H/'90
		- 10	100		100 uA	L-POWER		
		- 12	120					
		- 15	150					

DYNAMIC RAM

PROCESS	ORG	TYPE NO.	ACCESS TIME (MAX ns)	POWER ACTIVE	POWER S/B	FEATURE	PACKAGE (MIL)	AVAILABLE
NMOS	256K x 1	GM71256 - 10	100 ns	70 mA	4.5 mA	PAGE MODE	16 DIP	NOW
		- 12	120	65				
		- 15	150	60				
CMOS		GM71C256 - 80	80	60	3 mA	FAST PAGE MODE	16 DIP	1Q/'90
		- 10	100	50				
		- 12	120	45				
	64K x 4	GM71C464 - 80	80	60	3 mA	FAST PAGE MODE	18 DIP	1Q/'90
		- 10	100	50				
		- 12	120	45				
	1Mx1	GM71C1000 - 80	80 ns	70 mA	2 mA	FAST PAGE MODE	18 DIP 20 SOJ 20 ZIP	1H/'90
		- 10	100	60				
		- 12	120	50				
	256K x 4	GM71C4256A- 80	80 ns	66 mA	2 mA	FAST PAGE MODE	20 DIP 20 SOJ 20 ZIP	1H/'90
		- 10	100	55				
		- 12	120	47				
		GM71C4256 - 85	85 ns	95 mA	3 mA	FAST PAGE MODE	20 DIP 20 SOJ 20 ZIP	4Q/'89
		- 10	100	75				
		- 12	120	65				
		- 15	150	55				

MULTI PORT VIDEO RAM

PROCESS	ORG	TYPE NO.	ACCESS TIME (MAX ns)	POWER		FEATURE	PACKAGE (MIL)	AVAILABLE
				ACTIVE	S/B			
CMOS	64K x 4	GM53C461 - 80 - 10 - 12	80 ns 100 120	70 mA 60 50	6 mA	FAST PAGE MODE	24 ZIP	1H/'90

MASK ROM

NMOS	128K x 8	GM231000 - 25	250 ns	100 mA	20 mA		28 DIP	NOW
		GM231000 - 30A - 31A - 32A	250 ns	100 mA	20 mA	KOREAN/ CHINESE CHAR.	28 DIP	NOW

STATIC RAM

GoldStar	HITACHI	TOSHIBA	NEC	FUJITSU	OKI
GM76C28	HM6116/L	TC5517	uPD446	MB8416	MSM5128
GM76C88	HM6264	TC5565	uPD4364	MB8454	MSM5165
GM76C88L	HM6264L		uPD4364L	MB8464L	
GM56C88		TMM2088	uPD4363C	MB81C78A	
GM56C164	HM6788		uPD4362C	MB81C74	
GM76C256/L	HM62256	TC55257A	uPD43256	MB84256	M5M51257

DRAM

GoldStar	HITACHI	TOSHIBA	NEC	FUJITSU	OKI
GM71256	HM50256	TMM41256	uPD41256	MB81256	MSM41256A
GM71C256	HM51256			MB81C256	
GM71C464	HM50464P	TMM41464A	uPD41464	MB81464	M5M4464
GM71C4256	HM514256	TC514256	uPD424256	MB81C4256	MSM514256
GM71C1000	HM511000A	TC511000	uPD421000	MB81C1000	MSM511000
GM71C4256A	HM514256A	TC514256	uPD424256	MB81C4256	MSM514256

MULTI PORT VIDEO RAM

GoldStar	HITACHI	TOSHIBA	NEC	FUJITSU	AMD
GM53C461	HM53461			MB81461	AM90C644

MASK ROM

GoldStar	HITACHI	TOSHIBA	NEC	FUJITSU	OKI
GM231000	HN62301	TC531000	uPD23C1000	MB831000	MSM531000

MITSUBISHI	MOTOROLA	VITELIC	CYPRESS	SEIKO-EPS
M5M5117	MCM6116	V61C16	CY7C128	SRM2016
M5M5165	MCM6164	V62C64		
	MCM60L64	V62C64L		SRM2064
M5M5178	MCM6164C	V61C64	CY7C185L	
M5M5188A		V61C62	CY7C164	
M5M5256A	MCM60256	V62C256	CY7C198	SRM20256

MITSUBISHI	MOTOROLA	VITELIC	MICRO-T	TI
M5M4256A	MCM6255B	V53C256	MT1256	TMS4256
	MCM6256	V53C256		
M5M4464A	MCM4146A	V53C464		TMS4464
M5M44C256	MCM51426	V51C104	MT4C4256	TMS44C256
M5M4C1000			MT4C1024	TMX4C1024
M5M44C256			MT4C4256	TMS44C256

MITSUBISHI	MICRO-T	VITELIC	TI	IDT
M5M4C264	MT42C4064	V53C261	TMS461	

MITSUBISHI	SMI	MOTOROLA	MOSTEK	SIGNETICS
M5M23C100	SM231024			

A. TERMS AND DEFINITIONS

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level with the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

V_{DD} V_{CC}, V_{PP} Supply Voltage
The voltages supplied to the corrosponding voltage pins that are required for the device to the function.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current
The current flowing* the output with a specified high-level output voltage V_{OH} applied.

I_{OL} Low-level output current
The current flowing * the output with a specified low-level output voltage V_{OL} applied.

* Current flowing out of a terminal is a negative value.

$I_{O(off)}$ Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CC},I_{DD} Supply Current
The current into, respectively, the V_{DD}, V_{CC} Supply terminal.

DYNAMIC CHARACTERISTICS

t_A Access Time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example)

t_{ACC} address access time
t_{ACS} chip select access time
t_{OE} output enable access time

t_{XC} Cycle Time

The time interval between the start and end of a cycle.

Example)

t_{RC} Read cycle time
t_{WC} write cycle time

t_{SU} Setup Time

The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

Example)

t_{AS} address set-up time
t_{DW} input data set-up time
t_{ASW} write address set-up time

t_{HOLD} Hold Time

The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

Example)

t_{RAH} Row address hold time
t_{DH} Input data hold time
t_{ROH} Output data hole time from RAS

t_W Pulse Duration (width)

The time interval between specified reference points on the leading and trailing edges of the pules waveform.

Example)

t_{WP} Write pulse duration
t_{SP} Chip select pulse width

t_{REF} Refresh time interval

The time interval between the beginings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example)

t_{REF} Refresh time interval

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

The time interval in which output data contines to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Enable time (of a three-state output)

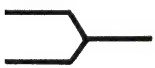
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, which the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

B. WAVEFORMS

Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	N/A	HIGH IMPEDANCE

ORDERING INFORMATION

GOLDSTAR MEMORY ORDERING INFORMATION

GM XXXXX XX — XX / XX XX

PERFIX OF GOLDSTAR MEMORY IC

PART NO

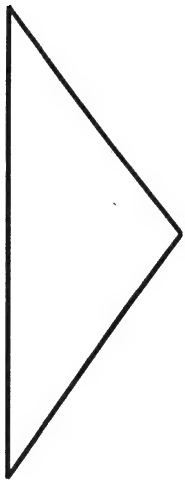
PACKAGE TYPE
BLANK : PLASTIC
D : CERDIP
C : SIDE-BRAZED
F : FLAT PACKAGE (SOP)
F (PACKAGE WIDTH :0.3 INCH)
FW (PACKAGE WIDTH :0.33 INCH)
SJ : SOJ
Z : ZIP
L : LEADLESS CHIR CARRIER
PL : PLASTIC LEADED CHIP CARRIER
S : SIP
G : PIN GRID ARRAY
K : SHRINK DIP
Y : SKINNY DIP(SLIM PACKAGE)
M : MODULE
X : DICE

SPEED

25:25ns	85: 85ns
35:35ns	10:100ns
45:45ns	12:120ns
55:55ns	15:150ns
60:60ns	20:200ns
70:70ns	25:250ns
80:80ns	30:300ns

BURN IN (OPTION)
B : BURN IN

TEMPERATURE RANGE (OPTION)
BLANK: COMMERCIAL
M : MILITERY
I : INDUSTRIAL



PRODUCT SPECIFICATION

GM76C28

CMOS 16K-BIT STATIC RAM

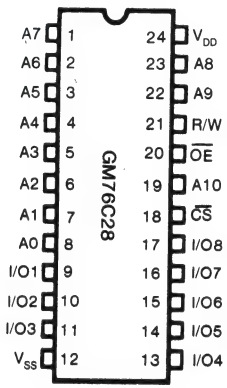
Description

The GM76C28$_{10/12}$ is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

Features

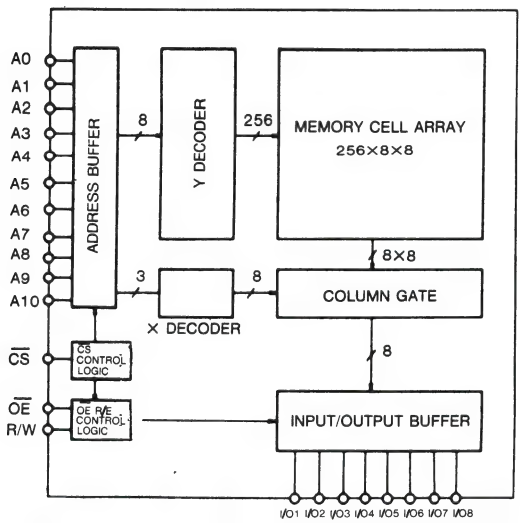
- **Access time ..... GM76C28-10 100ns(Max)**
  GM76C28-12 120ns(Max)
- **Low supply current ..... standby : 1μA(Typ)**
  operation: GM76C28-10 30mA(Typ)
  GM76C28-12 25mA(Typ)
- **Complete static operation**
- **Single power supply ..... 5V±10%**
- **TTL compatible inputs and outputs**
- **3-state output with wired-OR capability**
- **Non-volatile storage with back-up batteries**
- **Standard 24 DIP (600mil)/24 SOP (330mil)**

Pin Configuration



A0 to A10	Address Input
R/W	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply(+5V)
V_{SS}	Power Supply(0V)

Schematic Diagram



Absolute Maximum Ratings

Voltage on Any Pin with respect to GND	V_{DD}	−0.5 to 7.0V
Storage Temperature	T_{STG}	−65°C to +150°C
Operating Temperature	T_{OPR}	0°C to +70°C
Power dissipation	P_D	1.0W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

T_A=0°C to +70°C

V_{DD} Supply Voltage	4.5 to 5.5V
V_{IH} Input High Voltage	2.2 to 6.0V
V_{IL} Input Low Voltage	−0.5 to 0.8V

All voltages are referenced to GND pin=0V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics

DC Electrical Characteristics (V_{DD}=5V±10%, V_{SS}=0V, T_a=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	GM76C28-10			GM76C28-12			UNIT
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
I_{LI}	Input leakage current	V_{DD}=5.5V, V_I=0 to V_{DD}	−1		1	−1		1	μA
I_{LO}	Output leakage current	$\overline{CS}$=V_{IH}, or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	−1		1	−1		1	μA
I_{DDO}	Operating supply current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA		30	60		25	50	mA
I_{DDO1}		V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA		16			16		mA
I_{DDA}	Average operating current	Min. cycle, duty=100%, $I_{I/O}$=0mA		30	60		25	50	mA
I_{DDS}	Standby supply current	$\overline{CS}$=V_{IH}		1.5	3.0		1.5	3.0	mA
I_{DDS1}		$\overline{CS}$=V_{DD}−0.2V		1	50		1	50	μA
V_{OL}	Output voltage	I_{OL}=4.0mA			0.4			0.4	V
V_{OH}		I_{OH}=−1.0mA	2.4			2.4			V

* Typical values are for reference, with V_{DD}=5V and Ta=25°C assumed

Terminal Capacitance (f=1MHz, Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	V_I=0V		4	6	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$=0V		6	8	pF

AC Electrical Characteristics:

Read Cycle (V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	GM76C28-10		GM76C28-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read cycle time	*1	100		120		ns
t_{ACC}	Address access time			100		120	ns
t_{ACS}	$\overline{CS}$ access time			100		120	ns
t_{CLZ}	$\overline{CS}$ output setup time	*2	10		10		ns
t_{OE}	$\overline{OE}$ access time	*1		55		60	ns
t_{OLZ}	$\overline{OE}$ output setup time	*2	5		10		ns
t_{CHZ}	$\overline{CS}$ output floating		0	40	0	40	ns
t_{OHZ}	$\overline{OE}$ output floating		0	40	0	40	ns
t_{OH}	Output hold time	*1	10		10		ns

Write Cycle: (V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

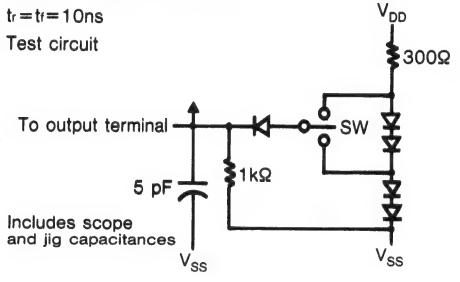
SYMBOL	PARAMETER	CONDITIONS	GM76C28-10		GM76C28-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write cycle time	*1	100	—	120	—	ns
t_{CW}	Chip select time ($\overline{CS}$)		80	—	85	—	ns
t_{AW}	Address enable time		80	—	85	—	ns
t_{AS}	Address setup time		0	—	0	—	ns
t_{WP}	Write pulse width		65	—	70	—	ns
t_{OHZ}	$\overline{OE}$ output floating	*2	0	40	0	40	ns
t_{WHZ}	R/W output floating	*3	0	45	0	50	ns
t_{DW}	Input data setup time	*1	45	—	50	—	ns
t_{WR}	Address hold time		5	—	5	—	ns
t_{DH}	Input data hold time		0	—	0	—	ns
t_{OW}	R/W output setup time	*3	5	—	10	—	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. t_r=t_f=10ns
3. Input/output timing reference level: 1.5V
4. Output load: 1 TTL+C_L=100pF

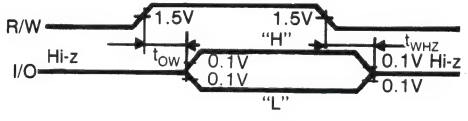
*3 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. t_r=t_f=10ns
3. Test circuit



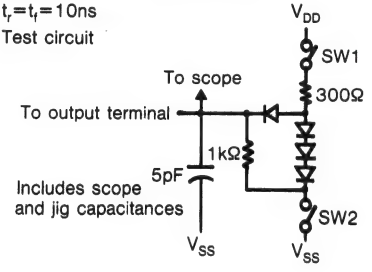
- o SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of low or t_{WHZ}
- o SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of low or t_{WHZ}

Output turnon turnoff times



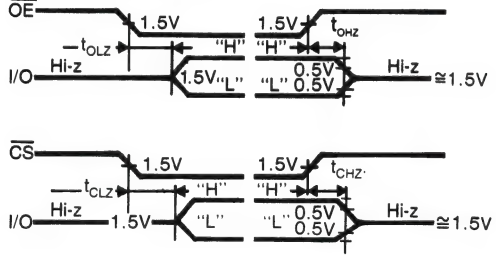
*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. t_r=t_f=10ns
3. Test circuit



- o Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OHZ}.
- o SW1 is open and SW2 is closed when measuring Hi-z-high of t_{CLZ} or t_{CLZ}
- o SW1 is closed and SW2 is open when measuring Hi-z-low t_{CLZ} or t_{CLZ}

Output turnon turnoff times



Functions

Truth Table

$\overline{CS}$	$\overline{OE}$	R/W	A0 to A10	DATA I/O	MODE	I_{DD}
H	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDSI}
L	L	H	Stable	Output data	Read	I_{DDO}
L	H	L	Stable	Input data	Write	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X: "H" or "L",—: "H", "L" or "Hi-Z"

Reading Data

Data can be read out if an address is set while $\overline{CS}$ and $\overline{OE}$ are held low, and R/W is held high.

Writing Data

There are following three ways of writing data.
(1) Hold $\overline{CS}$ low, set the address, and apply a low pulse to R/W.
(2) Hodl R/W low, set the address, and apply a low pulse to $\overline{CS}$.
(3) Set the address, then apply low pulses to both $\overline{CS}$ and R/W.
In any case, data from the DATA I/O terminal is fetched into the $GM76C28_{10/12}$ at the transition of a section in which both $\overline{CS}$ and R/W are low. Because the DATA I/O terminal is in high-impedance state when $\overline{CS}$ or $\overline{OE}$ is high, or R/W is low, contention of data driver on the bus and memory output is avoided.

Standby Mode

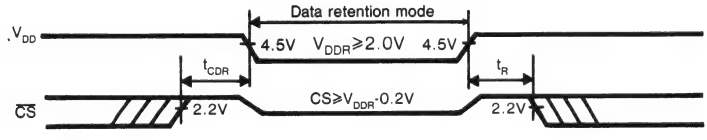
When $\overline{CS}$ is high, GM76C28 is in standby mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state and input of an address, R/W signal, or data is prohibited. When $\overline{CS}$ is above V_{DD}-0.2V, current flow within the GM76C28 chip is only that in the high-resistance portion of memory cells and leakage current.

Data Retention Characteristics with Low Voltage Power Supply (Ta=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDR}	Data retentions supply voltage	$\overline{CS} \geq V_{DDR}$-0.2V	2.0	—	5.5	V
I_{DDR}	Data retention current	V_{DD}=3.0V, $\overline{CS} \geq$2.8V	—	—	25	μA
t_{CDR}	Chip select data hold time	Refer to the figure below	0	—	—	ns
t_R	Operation recovery time		t_{RC}*	—	—	ns

* t_{RC}: read cycle time

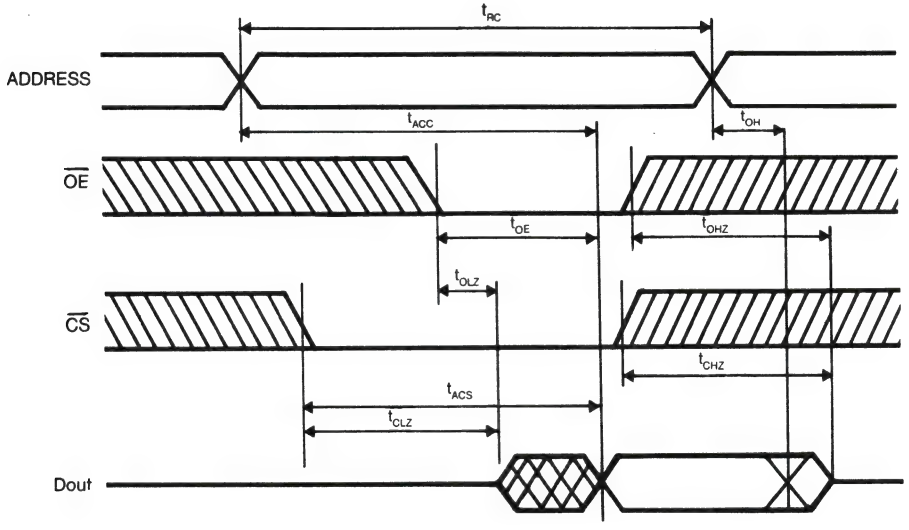
Data retention timing



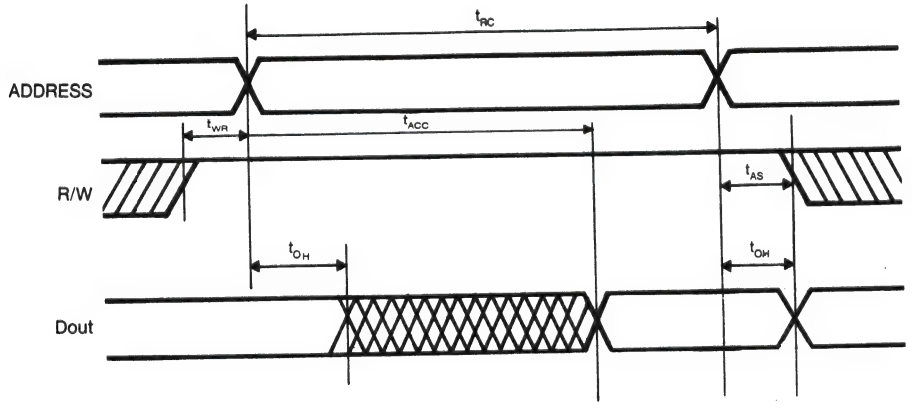
Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

Timing Chart

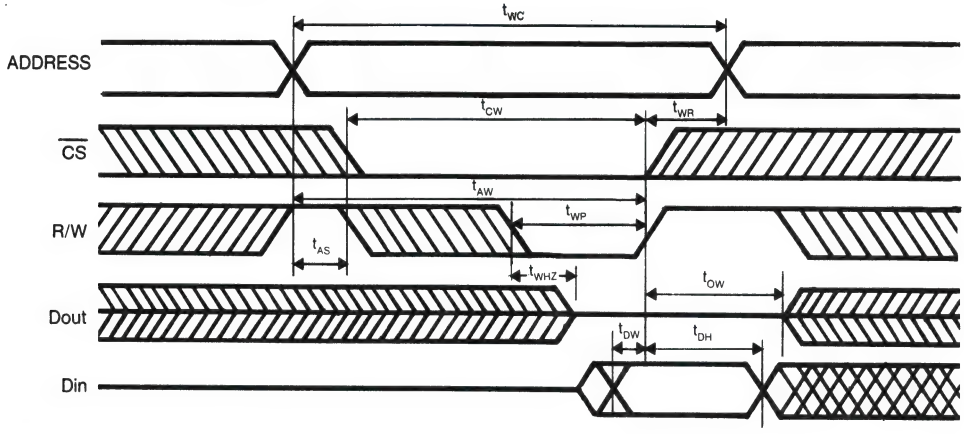
Reade cycle 1 ($\overline{OE}$, $\overline{CS}$ control, R/W=high)



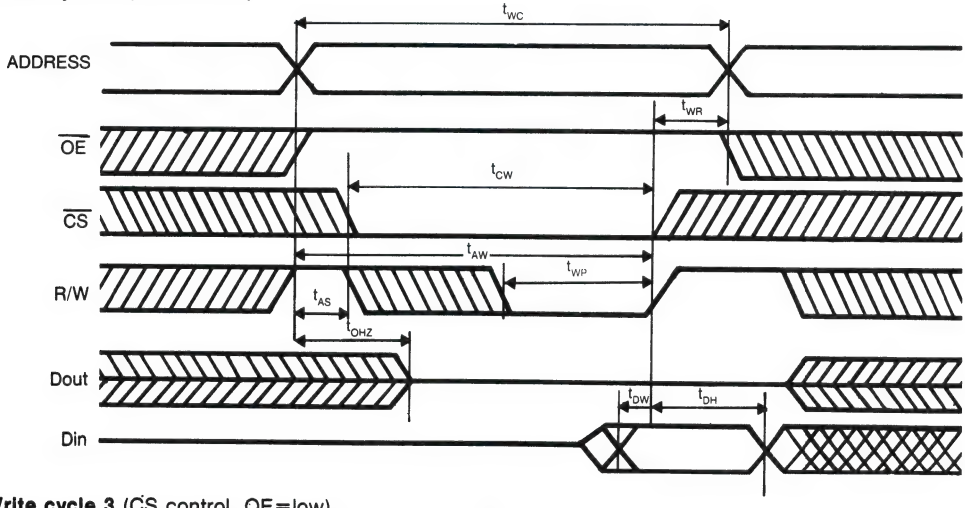
Read cycle 2 (R/W control, $\overline{OE}$=low, $\overline{CS}$=low)



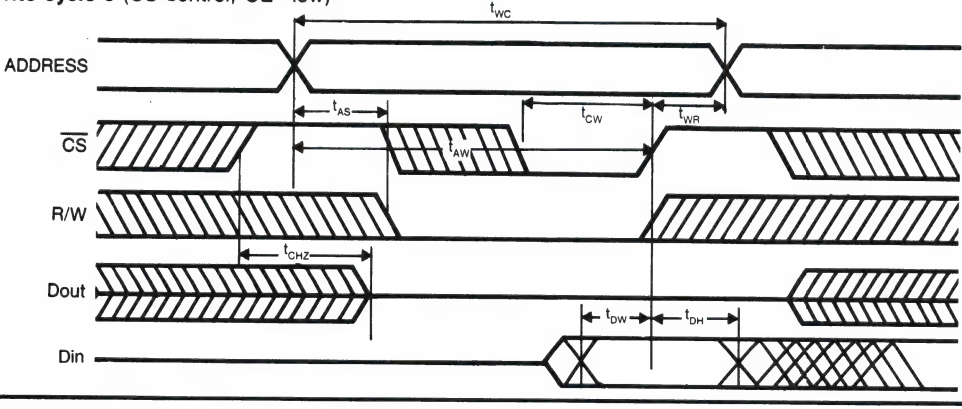
Write cycle 1 (R/W control, $\overline{OE}$=low)



Write cycle 2 (R/W control)

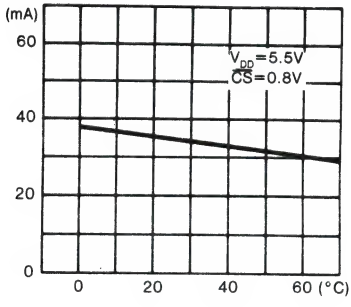


Write cycle 3 ($\overline{CS}$ control, OE=low)

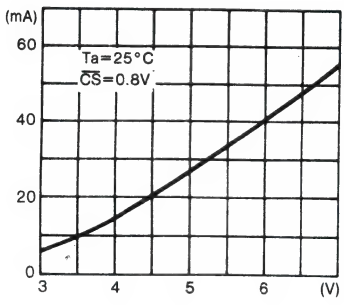


Characteristics Curves

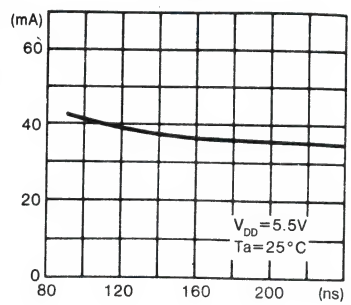
I_{DDO}-Ta



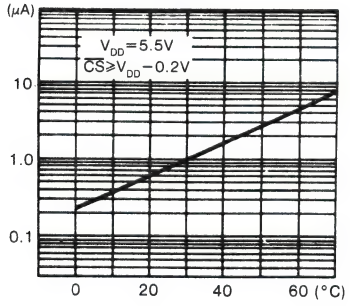
I_{DDO}-V_{DD}



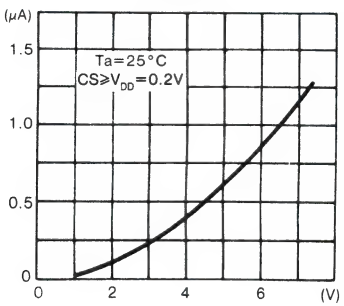
I_{DDA}-t_{cyc}



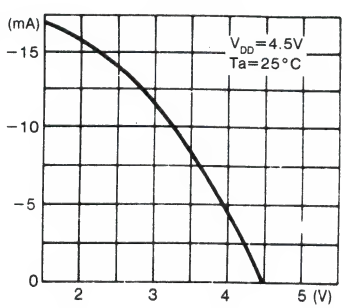
I_{DDSI}-Ta



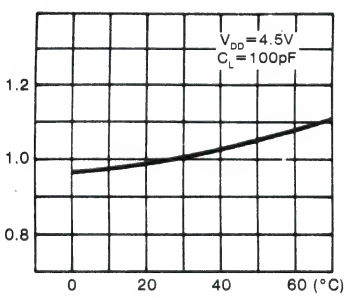
I_{DDSI}-V_{DD}



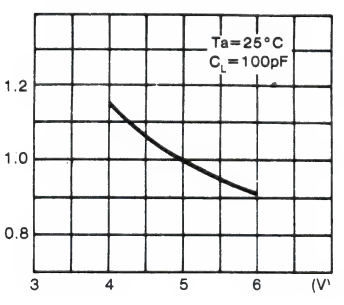
I_{OH}-V_{OH}



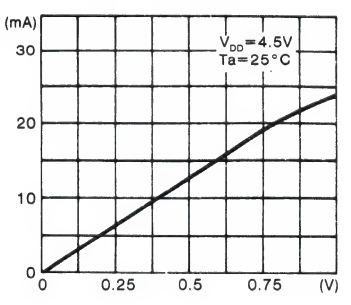
Normalized t_{ACC}·t_{ACS}·t_{OE}-Ta



Normalized t_{ACC}·t_{ACS}·t_{OE}-V_{DD}



I_{OL}-V_{OL}



PRODUCT SPECIFICATION

GM76C88

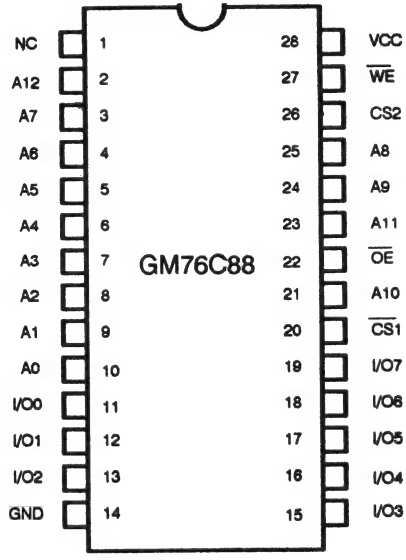
8,192 x 8 BIT STATIC RAM

Description

The GM76C88 is a high speed CMOS static RAM organized as 8,192x8 bits. It is manufactured using GSS's high performance CMOS technology.
Access times as fast as 85/100/120 ns are available with a maximum operating current of 80mA.
The GM76C88 features fully static operation requiring no external clocks or timing strobes.
Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), and active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the GM76C88 are TTL compatible and operate from single 5V supply thus simplifying system design.
The GM76C88 is processed following the test methods of MIL STD 883C.

Pin Configuration

(Top View)



Features

- 8,192 x 8 organization
- High Speed.
  Fast Access and Cycle Time 85/100/120 ns (Max.)
- Low Power Standby and Low Power Operation
  ACTIVE : 60mA (Typ)
  STANDBY : 20μA (Typ)
- Completely Static RAM : No Clock or Timing Strobe Required
- Common I/O (Three-State Output)
- Directly TTL Compatible : All Inputs and Outputs
- Single +5V Operation (±10%)
- Standard 28 DIP (600mil)

Pin Name

$A_0 \sim A_{12}$	: Address Input
$\overline{WE}$	: Write Enable Input
$\overline{OE}$	: Output Enable Input
$\overline{CS1}$, CS2	: Chip Select Input
$I/O_0 \sim I/O_7$	: Data Input/Output
V_{CC}	: Power Supply, +5V
GND	: Ground
NC	: No Connection

Absolute Maximum Ratings

Supply voltage to GND potential :	-2.0V to +7.0V
DC input voltage :	-0.5V to +7.0V
DC output voltage in high Z state :	-0.5V to +7.0V
Storage temperature :	-55°C to +150°C
Operating Temperature :	0°C to +70°C
Power dissipation :	1.0W

Recommended Operating Conditions:

T_A = 0°C to 70°C

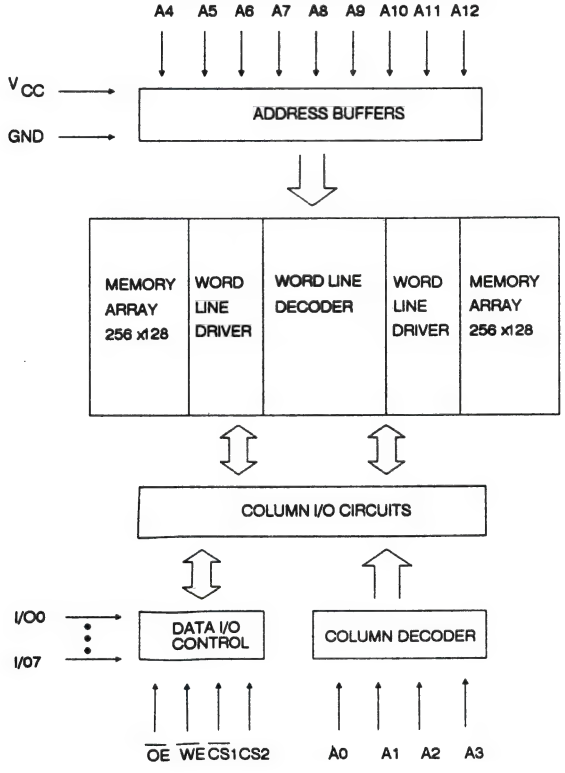
V_{CC} Supply Voltage	4.5 to 5.5V
V_{IH} Input High Voltage	2.2 to 6.0V
V_{IL} Input Low Voltage	-0.5 to 0.8V

All voltages are referenced to GND pin = 0V

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or elec tric fields; however, it is advised that normal precau tions be taken to avoid application of any voltage hig her than maximum rated voltages to this high-impe dance circuit.

Functional Block Diagram



Truth Table

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	MODE	I/O PIN	V_{CC} CURRENT	NOTE
X	X	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	L	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X : Don't Care

DC Electrical Characteristics: (V_{CC} = 5V ±10%, T_A = 0° ~ 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP*	MAX	UNIT
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-5	-	+5	μA
I_{LO}	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}	-10	-	+10	μA
I_{CC}	Power Supply Current	$\overline{CS1}$ = V_{IL}, $I_{I/O}$ = 0mA, CS2 = V_{IH}	-	40	80	mA
I_{CC}	Average Operating Current	MIN. cycle, duty = 100%, $I_{I/O}$ = 0mA, V_{CC} = MAX.	-	60	110	mA
I_{SB}	Standby Power Supply Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	-	1	3	mA
I_{SB1}		$\overline{CS1}$ ≥ VCC-0.2V, CS2 ≥ VCC-0.2V or CS2 ≤ 0.2V	_	0.02	2	mA
I_{SB2}		CS2 ≤ 0.2V	_	0.02	2	mA
V_{OL}	Output Voltage	I_{OL} = 2.1mA	_	_	0.4	V
V_{OH}		I_{OH} = -1.0mA	2.4	-	-	V

* Typical limits are at V_{CC} = 5.0V, T_A = 25°C and specified loading.

Capacitance : (T_A = 25°C, f = 1MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_I = 0V	-	6	pF
C_{OUT}	Output Capacitance	V_O = 0V	_	8	

Note : This parameter is sampled and not 100% tested.

AC Operating Characteristics: V_{CC} = 5V ± 10%, T_A = 0°C ~ 70°C

• Read Cycle

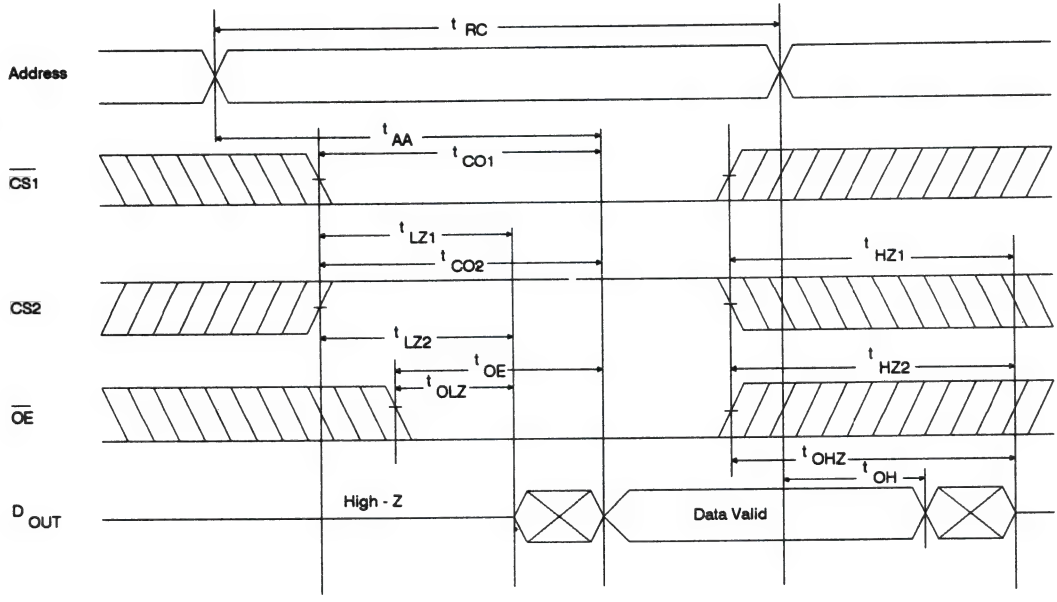
SYMBOL	PARAMETER		GM76C88-85		GM76C88-10		GM76C88-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time		85		100	_	120	_	ns
t_{AA}	Address Access Time		_	85	_	100	_	120	ns
t_{CO1}	Chip Selection to Output	$\overline{CS1}$	_	85	_	100	_	120	ns
t_{CO2}		CS2	_	85	_	100	_	120	ns
t_{OE}	Output Enable to Output Valid		_	40	_	50	_	60	ns
t_{LZ1}	Chip Selection to Output in Low Z	$\overline{CS1}$	10	_	10	_	10	_	ns
t_{LZ2}		CS2	10	_	10	_	10	_	ns
t_{OLZ}	Output Enable to Output in Low Z		5	_	5	_	5	_	ns
t_{HZ1}	Chip Deselection to Output in High Z	$\overline{CS1}$	0	35	0	35	0	40	ns
t_{HZ2}		CS2	0	35	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High Z		0	35	0	35	0	40	ns
t_{OH}	Output Hold from Address Change		10	_	10	_	10	_	ns

• Write Cycle

SYMBOL	PARAMETER		GM76C88-85		GM76C88-10		GM76C88-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time		85	_	100	_	120	_	ns
t_{CW}	Chip Selection to End of Write		70	_	80	_	85	_	ns
t_{AS}	Address Setup Time		0	_	0	_	0	_	ns
t_{AW}	Address Valid to End of Write		70	_	80	_	85	_	ns
t_{WP}	Write Pulse Width		50	_	60	_	70	_	ns
t_{WR1}	Write Recovery Time1	$\overline{CS1}$, $\overline{WE}$	5	_	5	_	5	_	ns
t_{WR2}	Write Recovery Time2	CS2	15	_	15	_	15	_	ns
t_{WHZ}	Write to Output in High Z		0	35	0	35	0	40	ns
t_{DW}	Data to Write Time Overlap		40	_	40	_	50	_	ns
t_{DH}	Data Hold from Write Time		0	_	0	_	0	_	ns
t_{OHZ}	$\overline{OE}$ to Output in High Z		0	35	0	35	0	40	ns
t_{OW}	Output Active from End of Write		5	_	5	_	10	_	ns

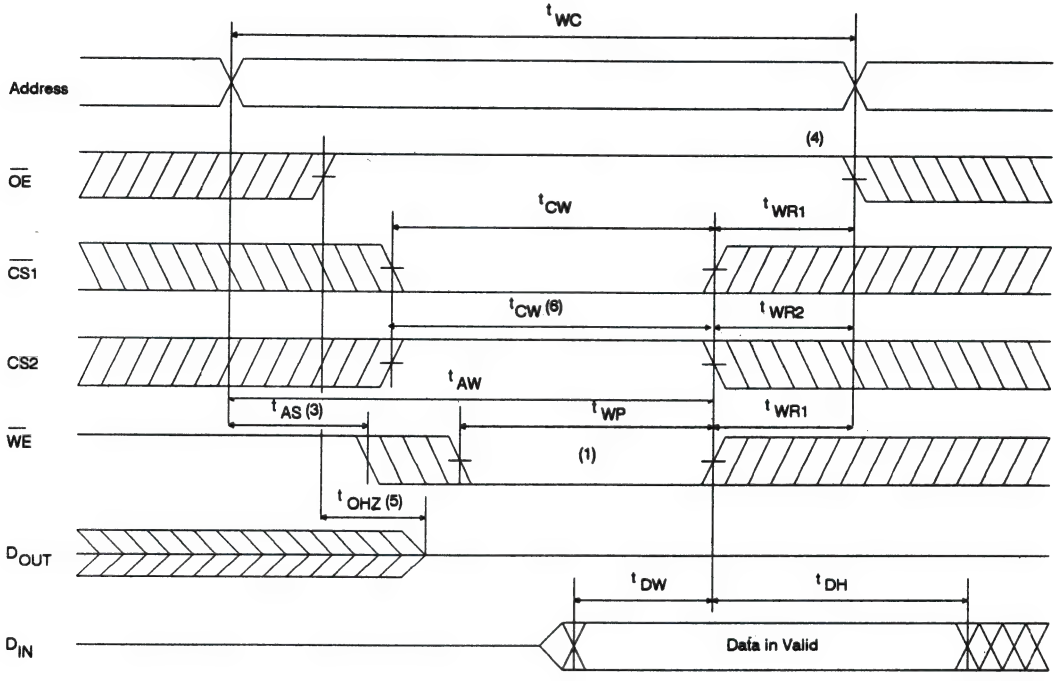
Timing Waveforms

•READ CYCLE (1)

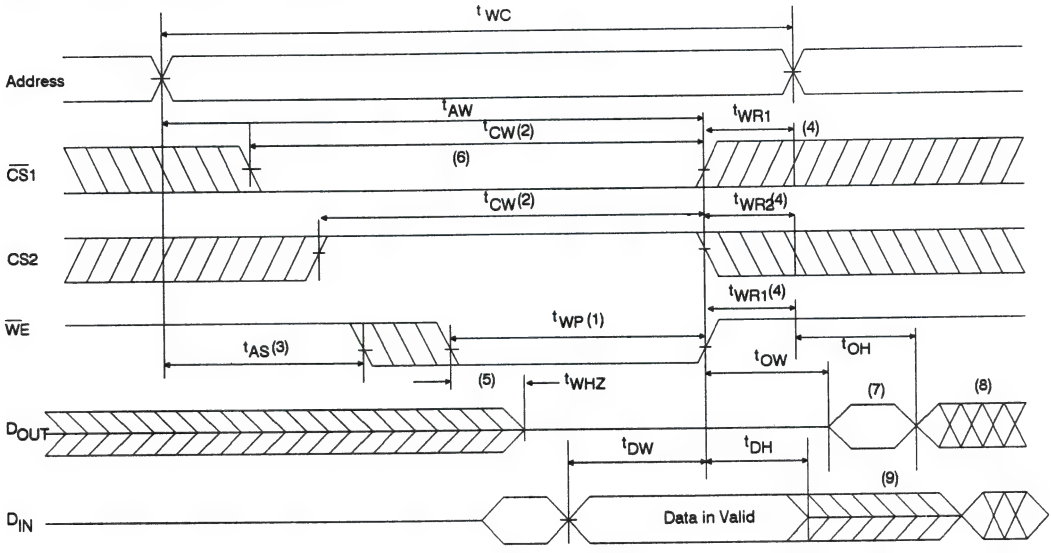


NOTE : 1 : $\overline{WE}$ is High for read cycle

•WRITE CYCLE (1) : ($\overline{OE}$ clock)



•WRITE CYCLE (2) : ($\overline{OE}$ Low Fix)

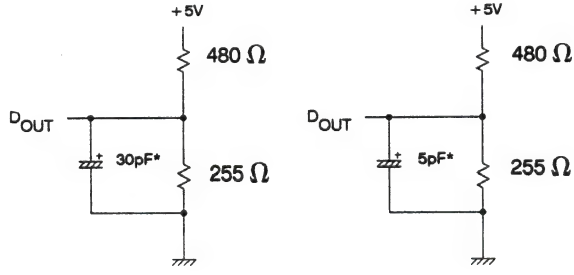


NOTES:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high. CS2 going low and $\overline{WE}$ going high tWP is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
   t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high
   t_{WR2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after WE going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10 nS
Input and Output Timing References	1.5 V
Output Load	1 TTL Gate and C_L = 100pF

Figure 1 Output Load **Figure 2 Output Load**
(for t_{LZ1}, t_{WHZ}, t_{OW})



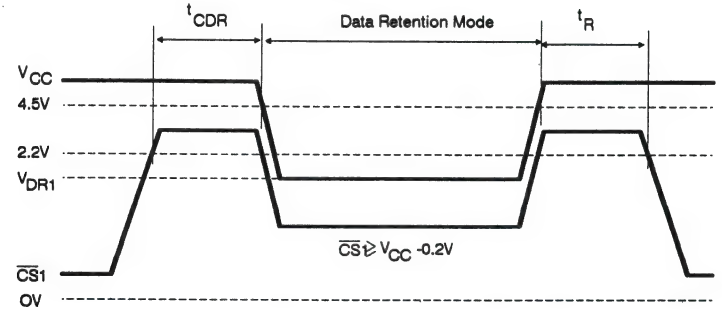
Data Retention Characteristics : (T_A = 0° ~ 70°C)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DR}	VCC for Data Retention	V_{DR1}	$\overline{CS1} \geq VCC-0.2V$, $CS2 \geq VCC-0.2V$ or $CS2 \leq 0.2V$	2.0	–	–	V
		V_{DR2}	$CS2 \leq 0.2V$	2.0	–	–	V
I_{CCDR}	Data Retention Current	I_{CCDR1}	$V_{CC}=3.0V$, $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq VCC-0.2V$ or $CS2 \leq 0.2V$	–	1	50*	μA
		I_{CCDR2}	$V_{CC}=3.0V$, $CS2 \leq 0.2V$	–	1	50*	μA
t_{CDR}	Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
t_R	Operation Recovery Time	t_R		t_{RC}**	–	–	ns

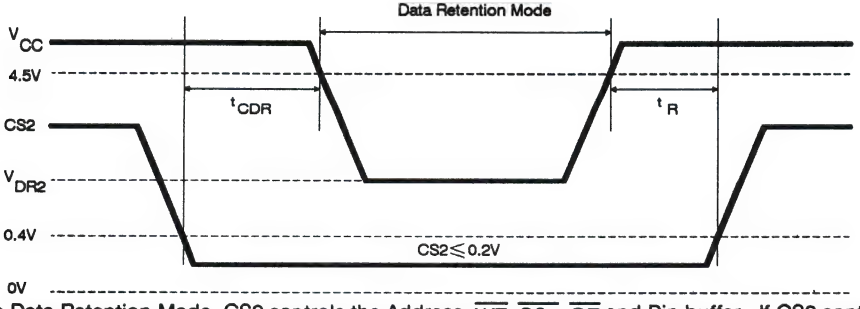
* V_{IL} min = -0.3V, 20μA max at T_A = 0 ~ 40°C

** t_{RC} = Read Cycle Time

• Low V_{CC} Data Retention Mode: (1) $\overline{CS1}$ Controlled



• Low V_{CC} Data Retention Mode: (2) CS2 Controlled



NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq VCC-0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

PRODUCT SPECIFICATION

GM76C88L

8,192 x 8 BIT STATIC RAM

Description

The GM76C88L is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology and operated from a single 5V supply. Advanced Circuit techniques provide low power feature with a maximum operating current of 40mA and stand by current of max. 100uA. Its very low stand by power requirment makes it idel for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no extrnal clock or refreshing circuits.

Features

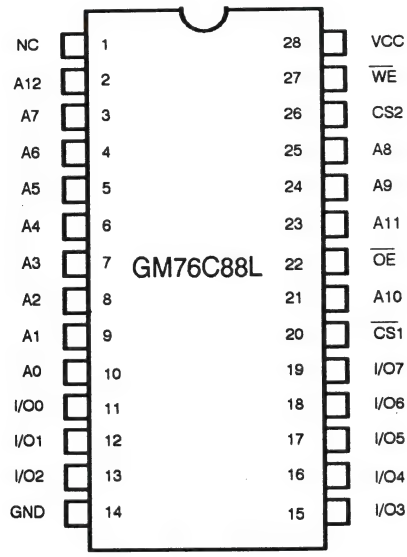
- 8,192 x 8 Organization
- Access Time : 150ns.
- Low Power Consumption
  : stand by 2uA (typ.)
  : operating 3mA/MHz (typ.)
- Completely Static RAM : No Clock or Timing Strobe Required
- Non-Volatile Storage with Back-Up Batteries
- 3-State Output with Wired-OR capability
- Directly TTL Compatible : All Inputs and Outputs
- Single +5V Operation (±10%)
- Standard 28 DIP and SOP capability

Ordering Information

TYPE NO.	ACCESS TIME	PACKAGE
GM76C88L-15	150 ns	600 MIL 28 Pin Plastic DIP
GM76C88LFW-15	150 nS	330 MIL 28 Pin SOP

Pin Configuration

(Top View)



Absolute Maximum Ratings

Supply Voltage	Vdd	-0.5 ~ 7.0V
Input Voltage	Vin	-0.5 ~ 7.0V
Powe Dissipation	Pd	1.0W
Operating Temperature	Topr	0 ~ 70°C
Storage Temperature	Tstg	-65 ~ 150°C
Soldering Tempeature and Time	Tsol	260°C,10s(at lead)

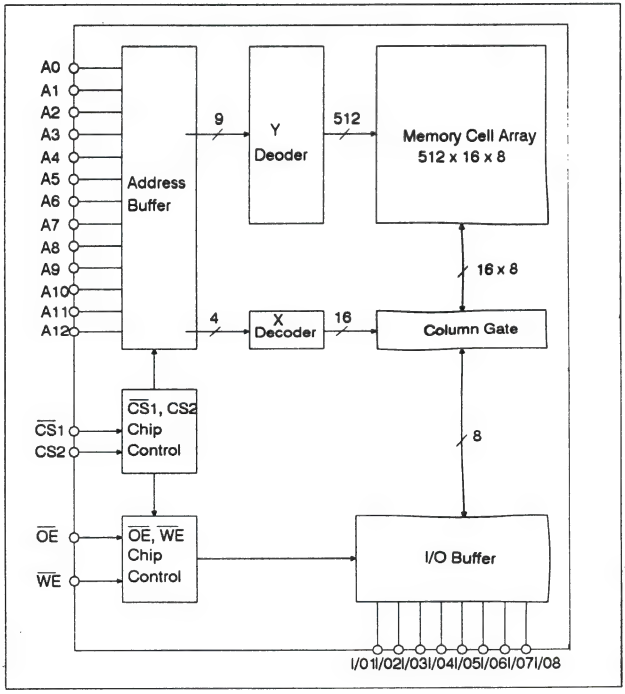
Recommended Operating Conditions:

TA = 0°C to +70°C	
V_{CC} Supply Voltage	4.5 to 5.5V
V_{IH} Input High Voltage	2.2 to 6.0V
V_{IL} Input Low Voltage	-0.5 to 0.8V
All voltage are referenced to GND pin = 0V	

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or elec tric fields; however, it is advised that normal precau tions be taken to avoid application of any voltage hig her than maximum rated voltages to this high-impe dance circuit.

Functional Block Diagram



DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0° ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS		GM76C88L-15			UNIT
				MIN	TYP*1	MAX	
I_{LI}	Input leakage current	V_I = 0 to V_{DD}		-1	_	1	μA
I_{DDS}	Standby supply current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}		_	1.5	3.0	mA
I_{DDSI}		$\overline{CS1}$ = CS2 ≥ VDD - 0.2V or CS2 ≤ 0.2V		_	2	100	μA
I_{DDA}	Average operating current	V_I = V_{IL}, V_{IH}	t_{CYC} = 1μs	_	6	10	mA
		$I_{I/O}$ = 0mA	t_{CYC} = Min	_	25	40	
I_{DDAI}		V_I = 0.2V V_{DD} = 0.2V $I_{I/O}$ = 0.2V	t_{CYC} = 1μs	_	3	5	mA
			t_{CYC} = Min	_	20	35	
I_{LO}	Output leakage current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{DD}		-1	_	1	uA
V_{OH}	High level output voltage	I_{OH} = -1.0mA		2.4	V_{DD}-0.1	_	V
V_{OL}	Low level output voltage	I_{OL} = 4.0mA		_	0.2	0.4	V

* 1 Typical values are for Ta = 25°C and V_{DD} = 5.0V

Capacitance : (T_A = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_I = 0V	-	6	pF
C_{OUT}	Output Capacitance	V_O = 0V	_	8	

Note : This parameter is sampled and not 100% tested.

AC Operating Characteristics : V_{DD} = 5V ± 10%, T_A = 0° ~ 70°C

•Read Cycle

SYMBOL	PARAMETER	CONDITIONS	GM76C88L-15		UNIT
			MIN	MAX	
t_{RC}	Read cycle time	* 1	150	_	ns
t_{ACC}	Address access time		_	150	ns
t_{ACS1}	Chip select 1 access time		_	150	ns
t_{ACS2}	Chip select 2 access time		_	150	ns
t_{OE}	Output enable access time		_	70	ns
t_{CLZ1}	Chip enable 1 output set time	* 2	10	_	ns
t_{CHZ1}	Chip enable 1 output floating		_	70	ns
t_{CLZ2}	Chip enable 2 output set time		10	_	ns
t_{CHZ2}	Chip enable 2 output floating		_	70	ns
t_{OLZ}	Output enable output set time		5	_	ns
t_{OHZ}	Output enable output floating time		_	60	ns
t_{OH}	Output hold time	* 1	30	_	ns

AC Operating Characteristics: V_{CC} = 5V ± 10%, T_A = 0°C ~ 70°C

• Write Cycle

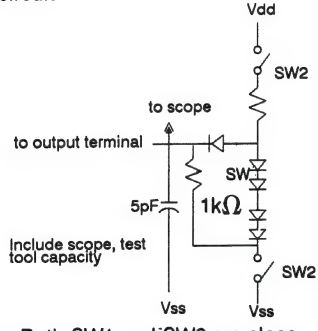
SYMBOL	PARAMETER	CONDITIONS	GM76C88L-15		UNIT
			MIN	MAX	
t_{WC}	Write cycle time	* 1	150	_	ns
t_{CW1}	Chip select time 1		120	_	ns
t_{CW2}	Chip select time 2		120	_	ns
t_{AW}	Address enable time		120	_	ns
t_{AS}	Address setup time		0	_	ns
t_{WP}	Write pulse width		100	_	ns
t_{WR}	Address hold time		0	_	ns
t_{DW}	Input data setup time		60	_	ns
t_{DH}	Input data hold time	* 3	0	_	ns
t_{WHZ}	R/W Output floating		_	70	ns
t_{OW}	R/W Output setup time		10	_	ns

* 1 Test Conditions

1. Input pulse level : 0.8V to 2.2V
2. tr = tf = 10ns
3. Input and output timing reference levels 1.5V
4. Output load 1_{TTL} + C_L = 100pF

* 2 Test Conditions

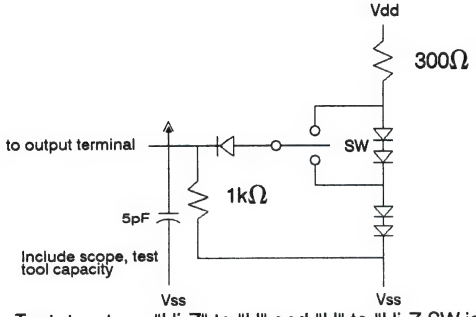
1. Input pulse level : 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit



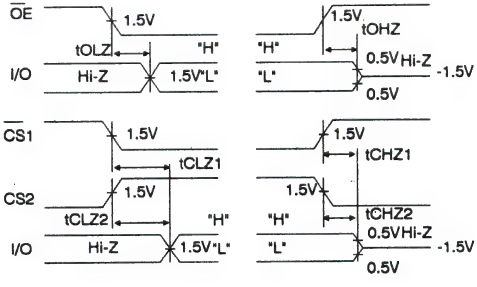
Test:t_{CHZ1},t_{CHZ2},t_{OHZ} Both SW1 and SW2 are close
Test:t_{CLZ1},t_{CLZ2},t_{OLZ} "Hi-Z" to "H" SW1 is open,SW2 is close.
Test:t_{CLZ1},t_{CLZ2},t_{OLZ} "Hi-Z" to "L" SW1 is close, SW2 is open.

* 3 Test Conditions

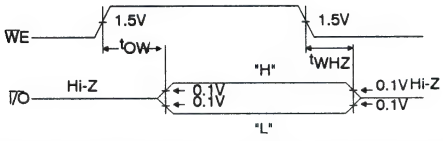
1. Input pulse level : 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit



Test: t_{OW},t_{WHZ} "Hi-Z" to "H" and "H" to "Hi-Z SW is V_{DD} side
Test: t_{OW},t_{WHZ} "Hi-Z to "L" and "L" to Hi-Z" SW is V_{SS} side



Output turnon turnoff time



FUNCTIONS

•Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A1 to A12	DATA I/O	MODE
H	X	_	_	_	Hi-Z	Unselected
_	L	_	_	_	Hi-Z	Unselected
L	H	X	L	Stable	Input data	Write
L	H	L	H	Stable	Output data	Read
L	H	H	H	Stable	Hi-Z	Output disable

X : "H" or "L". _ : "H", "L" or "Hi-Z"

•Reading data

Data is able to be read by setting addresses during holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". And as Data I/O terminals are high impedance when $\overline{OE}$ = "H", the data bus line can be used for any other object, then access time apparently is able to be cut down.

•Writing data

There are following four ways of writing data into memory.

(1) During holding CS2 = "H", $\overline{WE}$ = "L" set addresses and give "L" pulse to $\overline{CS1}$.

(2) During holding $\overline{CS1}$ = "L", $\overline{WE}$ set addresses and give "H" pulse to CS2.

(3) During holding $\overline{CS1}$ = "L", CS2 = "H" set addresses and give "L" pulse to $\overline{WE}$.

(4) After seting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

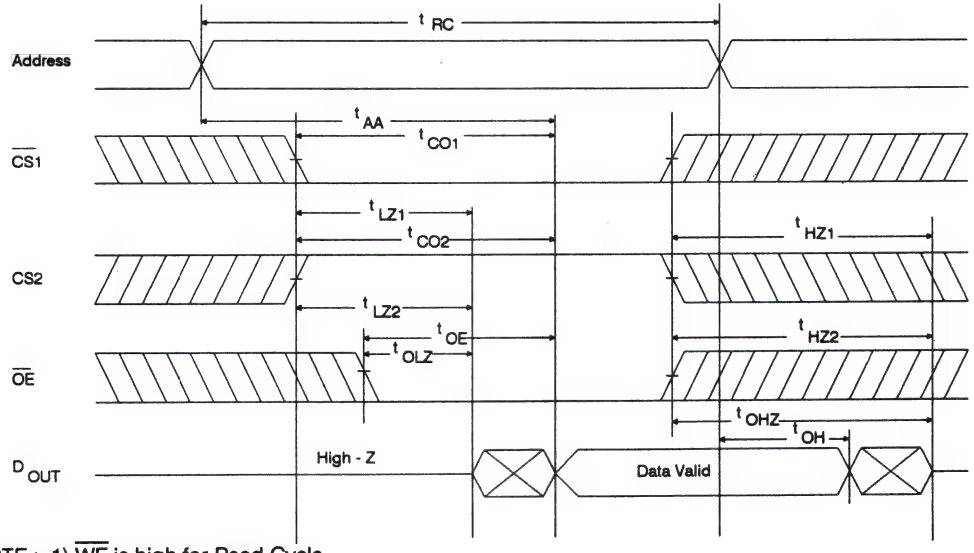
Anyway, data on the Data I/O terminals are latched up into the GM76C88L at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As Data I/O terminals are high impedance when any of $\overline{CS1}$, $\overline{OE}$ = "H", or CS2 = "L", the contention of data driver with memory output bus can be avoided.

•Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level the GM76C88L is in the standby mode and the operation is only retaining data. In this case Data I/O terminals are Hi-Z, and all inputs of address, $\overline{WE}$ and data are prohibited. When $\overline{CS1}$ and CS2 level are in the range over V_{DD}-0.2V, or CS2 level is in the range under 0.2V, in the GM76C88L there is almost current flow through the high resistance parts of the memory.

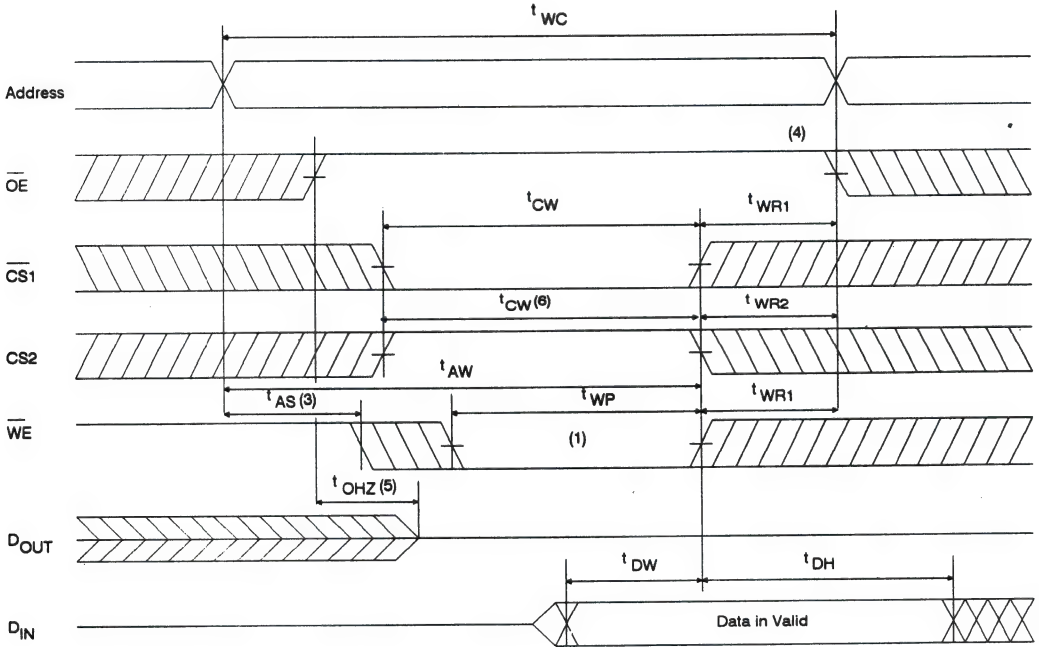
Timing Waveforms

•READ CYCLE

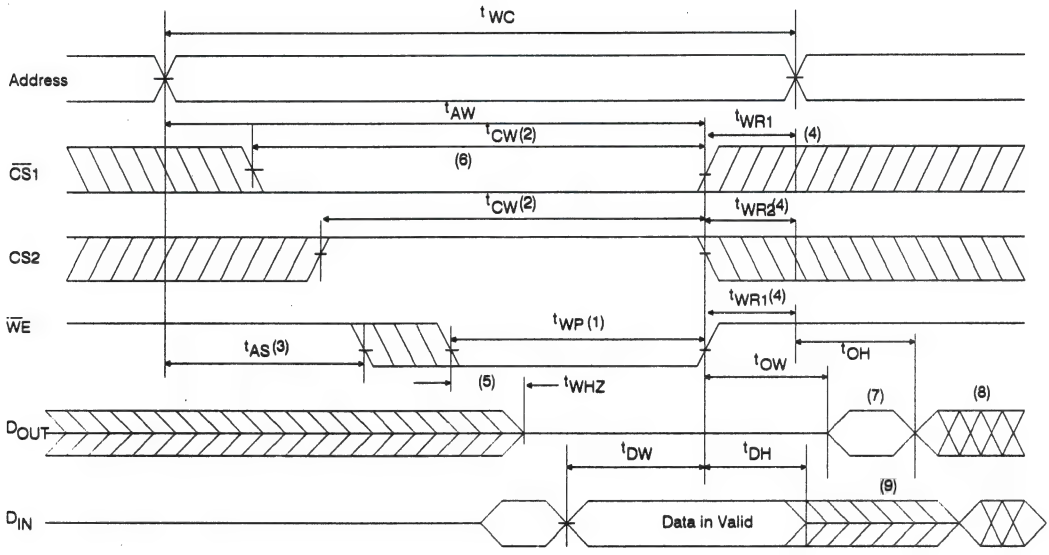


NOTE : 1) $\overline{WE}$ is high for Read Cycle

•WRITE CYCLE (1) ($\overline{OE}$ clock)



•WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES:
1. A write occurs during the overlap of a low CS1, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high. CS2 going low and $\overline{WE}$ going high tWP is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
   t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high
   t_{WR2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

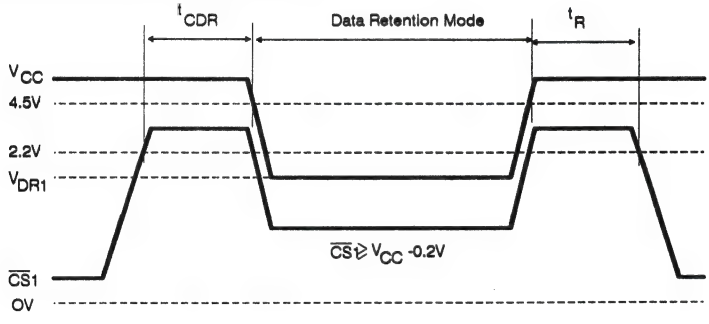
Data Retention Characteristics : (T_A = 0° ~ 70°C)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DR}	V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq$ VCC-0.2V, CS2 $\geq$ VCC-0.2V or CS2 $\leq$ 0.2V	2.0	–	–	V
		V_{DR2}	CS2 $\leq$ 0.2V	2.0	–	–	V
I_{CCDR}	Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geq V_{CC}$-0.2V, CS2 $\geq$ VCC-0.2V or CS2 $\leq$ 0.2V	–	1	50*	µA
		I_{CCDR2}	V_{CC} = 3.0V, CS2 $\leq$ 0.2V	–	1	50*	µA
t_{CDR}	Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
t_R	Operation Recovery Time	t_R		t_{RC}**	–	–	ns

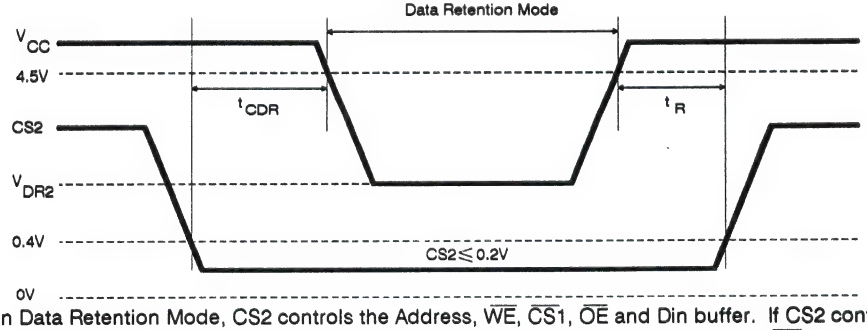
* V_{IL} min = -0.3V, 20µA max at T_A = 0 ~ 40°C

** t_{RC} = Read Cycle Time

•Low V_{CC} Data Retention Mode: (1) $\overline{CS1}$ Controlled



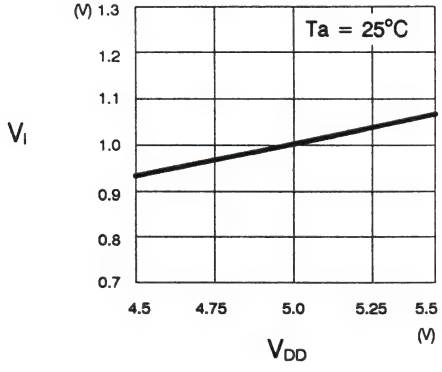
•Low V_{CC} Data Retention Mode: (2) CS2 Controlled



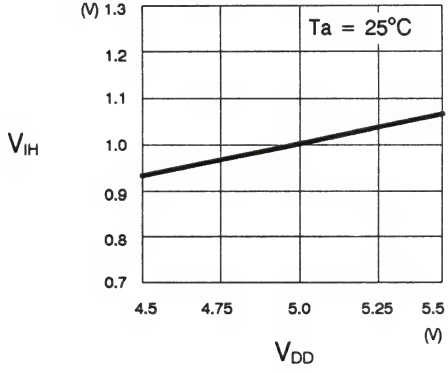
NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 $\geq$ VCC -0.2V or CS2 $\leq$ 0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

CHARACTERISTICS CURVES (Continued)

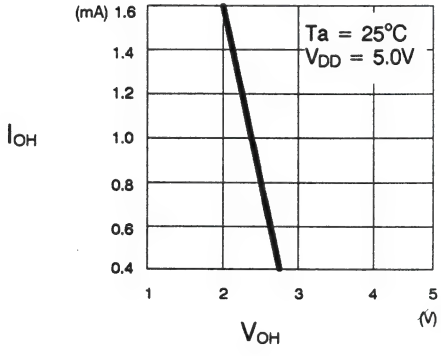
Normalized V_I - V_{DD}



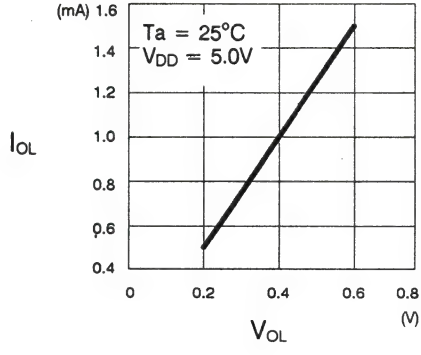
Normalized V_{IH} - V_{DD}



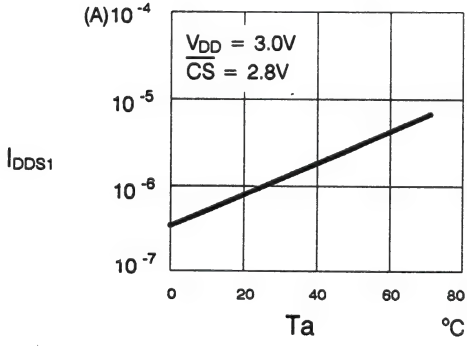
Normalized I_{OH} - V_{OH}



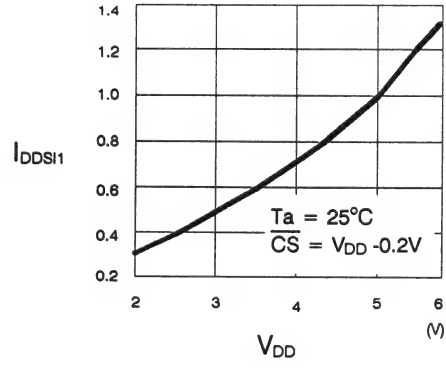
Normalized I_{OL} - V_{OL}



I_{DDS1} - Ta



Normalized I_{DDS1} - VDD



PRELIMINARY SPECIFICATION

GM56C88

HIGH SPEED CMOS SRAM

Description

The GM56C88 is a high speed CMOS static RAM organized as 8192x8 bits. It is manufactured using GSS's high performance CMOS technology.

Access times as fast as 35 ns are available with maximum power consumption of only 550mW.

The GM56C88 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73% when the circuit is deseleced.

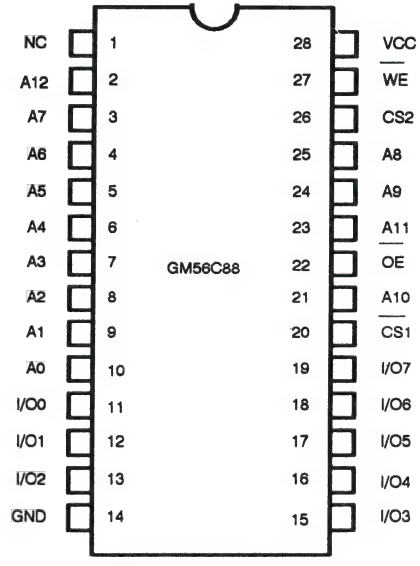
Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), and active low output enable ($\overline{OE}$) and three state drivers.

All inputs and outputs of the GM56C88 are TTL compatible and operate from single 5V supply thus simplifying system design.

The GM56C88 is processed following the test methods of MIL STD 883C.

Pin Configuration

(Top View)



Features

- 8,192 x 8 organization
- High Speed.
  Fast Access and Cycle Time 35/45/55 ns (Max.)
- Low Power Standby and Low Power Operation
  ACTIVE : 380mW (Typ)
  STANDBY : 110mW (Typ)
- Completely Static RAM : No Clock or Timing Strobe Required
- Common I/O (Three-State Output)
- Directly TTL Compatible : All Inputs and Outputs
- Single +5V Operation (±10%)
- Standard 28 DIP (300MIL)
- Capable of withstanding Greater than 2000V Electrostatic Discharge

Pin Name

$\overline{A_0} \sim A_{12}$	: Address Input
$\overline{WE}$	: Write Enable Input
$\overline{OE}$	: Output Enable Input
$\overline{CS1}$, CS2	: Chip Select Input
$I/O_0 \sim I/O_7$	: Data Input/Output
V_{CC}	: Power Supply, +5V
GND	: Ground

Absolute Maximum Ratings

Supply voltage to GND potential : -0.5V to +7.0V
DC input voltage : -3.0V to +7.0V
DC output voltge in high Z state : -0.5V to +7.0V
Storage temperature : -65°C to +150°C
Output Current into outputs (low) : 20mA
Electro static discharge voltage : >2000V (MIL STD 883C method 3015.2)

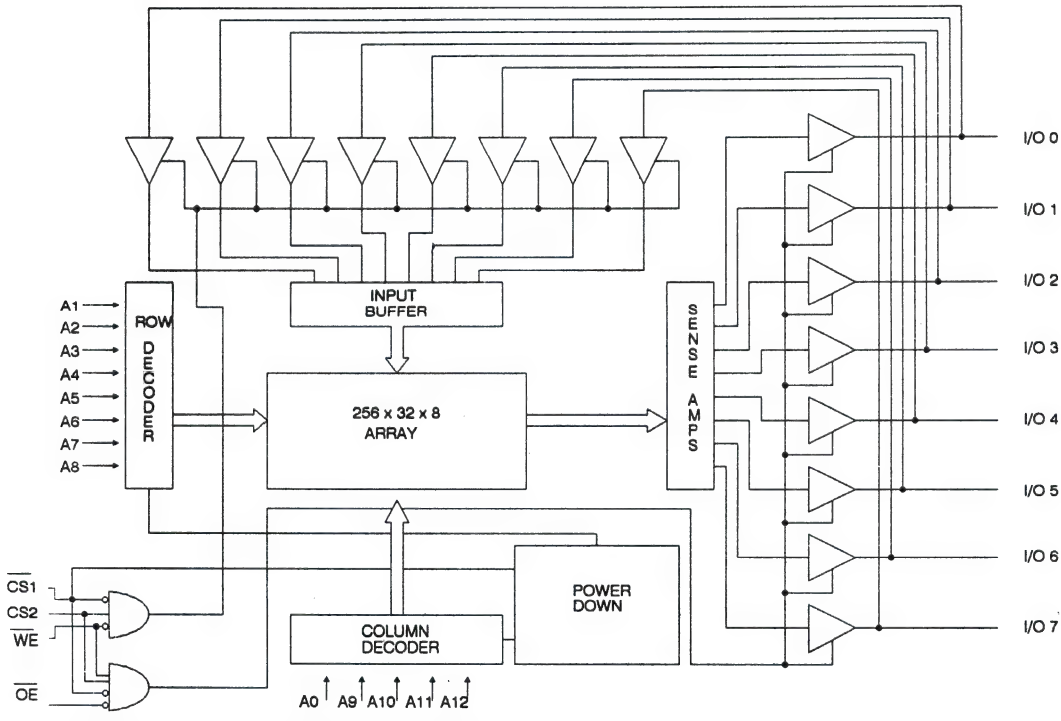
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions:

T_A = 0°C to 70°C	
V_{CC} Supply Voltage	4.5 to 5.5V
V_{IH} Input High Voltage	2.2 to V_{CC}
V_{IL} Input Low Voltage	-3.0 to 0.8V
All voltages are referenced to GND pin = 0V	

This device contains circuitry to protect the inputs against damage due to high static voltages or elec tric fields; however, it is advised that normal precau tions be taken to avoid application of any voltage hig her than maximum rated voltages to this high-impe dance circuit.

Functional Block Diagram



Truth Table

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	MODE	I/O PIN	V_{CC} CURRENT	NOTE
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}	
X	X	L	X		High Z	I_{SB}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X : Don't Care

DC Electrical Characteristics: (V_{CC} = 5V +10%, T_A = 0° ~ 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP*	MAX	UNIT
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-10	-	+10	μA
I_{LO}	Output Leakage Current	CS1 = V_{IH} or CS2 = V_{IL} or OE = V_{IH} or WE = V_{IL}, $V_{I/O}$ = GND to V_{CC}	-10	-	+10	μA
I_{OS}*2	Output Short Circuit Current	V_{CC} = MAX, Vout = GND	-	-	-300	mA
I_{CC}	Average Operating Current	MIN. cycle, duty = 100%, $I_{I/O}$ = 0mA, V_{CC} = MAX. V_{IN} = V_{CC} or GND	-	-	100	mA
I_{SB}	Standby Power Supply Current	CS1 ≥ V_{IH} or CS2 ≤ V_{IL}	-	-	30	mA
V_{OL}	Output Voltage	I_{OL} = 8.0mA	-	-	0.4	V
V_{OH}		I_{OH} = -4.0mA	2.4	-	-	V

* Typical limits are at V_{CC} = 5.0V, TA = 25°C and specified loading.

*2 Duration of the short circuit should not exceed 30 seconds.

Capacitance : (T_A = 25°C, f = 1MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_I = 0V	-	5	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	7	

Note : This parameter is sampled and not 100% trested,.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing References	1.5 V
Output Load (I_{OL}/I_{OH})	+30pF

including scope and jig.

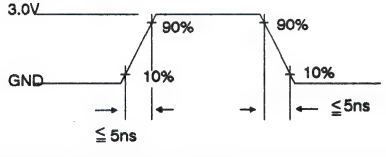


Figure 1 Output Load

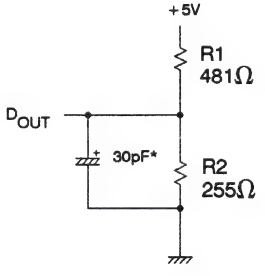
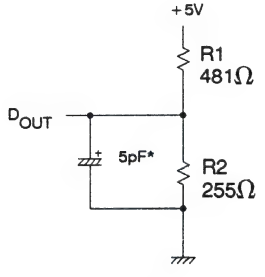


Figure 2 Output Load

(for t_{LZ1}, t_{WHZ}, t_{OW})



AC Operating Characteristics: V_{CC} = 5V ± 10%, T_A = 0°C ~ 70°C

• Read Cycle

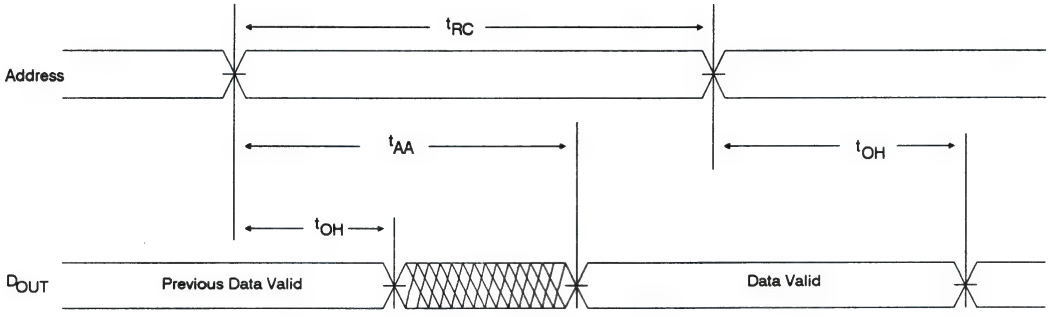
SYMBOL	PARAMETER		GM56C88-35		GM56C88-45		GM56C88-55		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time		35		45	_	55	_	ns
t_{AA}	Address Access Time		_	35	_	45	_	55	ns
t_{CO1}	Chip Selection to Output	$\overline{CS1}$	_	35	_	45	_	55	ns
t_{CO2}		CS2	_	25	_	30	_	40	ns
t_{OE}	Output Enable to Output Valid		_	20	_	20	_	25	ns
t_{LZ1}	Chip Selection to Output in Low Z	$\overline{CS1}$	5	_	5	_	5	_	ns
t_{LZ2}		CS2	3	_	3	_	3	_	ns
t_{OLZ}	Output Enable to Output in Low Z		3	_	3	_	3	_	ns
t_{HZ1}	Chip Deselection to Output in High Z	$\overline{CS1}$	0	15	0	20	0	20	ns
t_{HZ2}		CS2	0	15	0	20	0	20	ns
t_{OHZ}	Output Disable to Output in High Z		0	20	0	25	0	30	ns
t_{OH}	Output Hold from Address Change		3	_	3	_	3	_	ns
t_{PU}	$\overline{CS1}$ Low to Power Up		0	_	0	_	0	_	ns
t_{PD}	$\overline{CS1}$ High to Power Down		_	20	_	25	_	25	ns

• Write Cycle

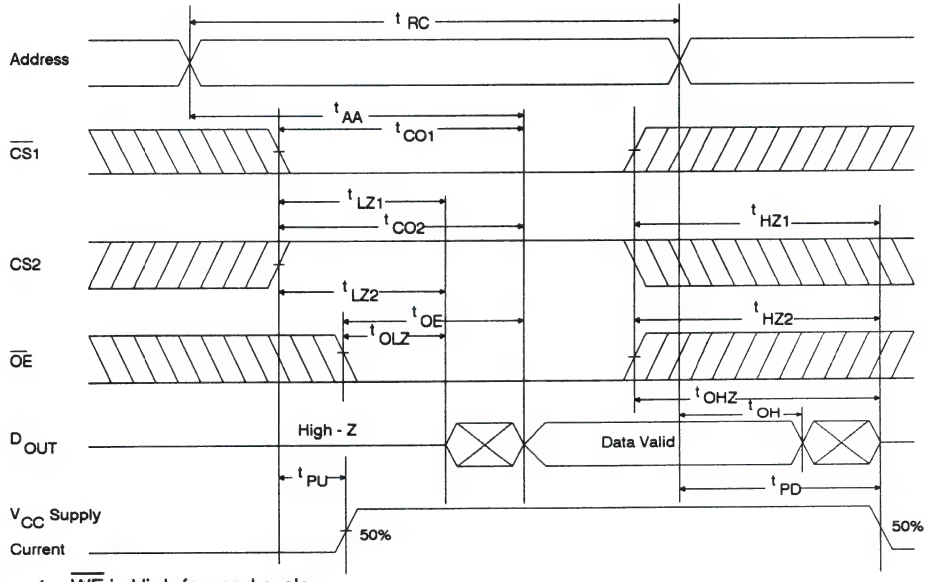
SYMBOL	PARAMETER	GM56C88-35		GM56C88-45		GM56C88-55		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	35	_	45	_	50	_	ns
t_{CW1}	$\overline{CS1}$ Low to Write End	30	_	40	_	50	_	ns
t_{CW2}	CS2 High to Write End	20	_	25	_	30	_	ns
t_{AS}	Address Setup Time	0	_	0	_	0	_	ns
t_{AW}	Address Valid to End of Write	30	_	40	_	50	_	ns
t_{WP}	Write Pulse Width	20	_	25	_	30	_	ns
t_{WR}	Write Recovery Time (Address Hold from end of Write)	0	_	0	_	0	_	ns
t_{WHZ}	Write to Output in High Z	0	15	0	20	0	25	ns
t_{DW}	Data to Write Time Overlap	15	_	20	_	25	_	ns
t_{DH}	Data Hold from Write Time	0	_	0	_	0	_	ns
t_{OW}	Output Active from End of Write	3	_	3	_	3	_	ns

Timing Waveforms

•READ CYCLE (1) : note (1, 2)

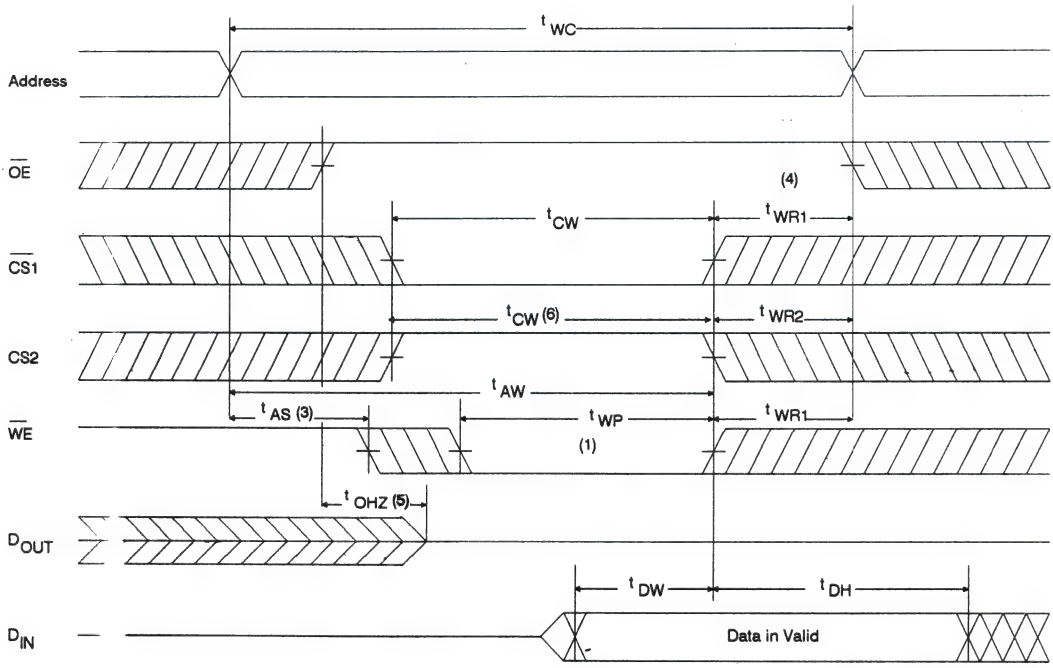


•READ CYCLE (2) : note (1, 3)

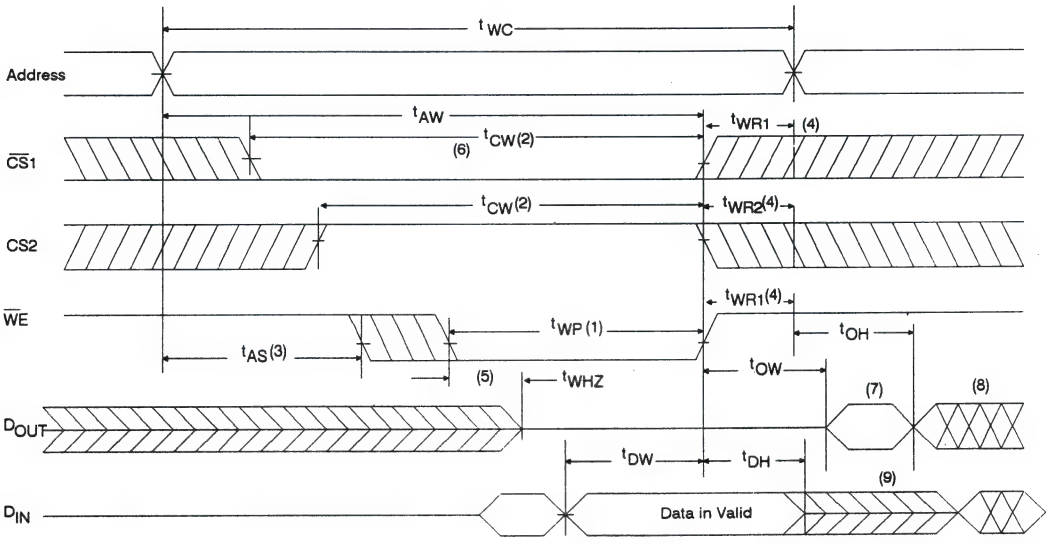


NOTE : 1 : $\overline{WE}$ is High for read cycle
2 : Device is continuously selected. $\overline{CS1}$/OE = V_{IL} and CS_2 = V_{IH}.
3 : Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE (1) : $\overline{WE}$ Controlled



• WRITE CYCLE (2) : $\overline{CS1}$ Controlled.



NOTES:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low WE. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low. A write ends at the earliest transition among $\overline{CS1}$ going high. CS2 going low and WE going high tWP is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
   t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high
   t_{WR2} applies in case a write ends at CS2 going low.
5. During this period. I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ goin low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

GM56C164

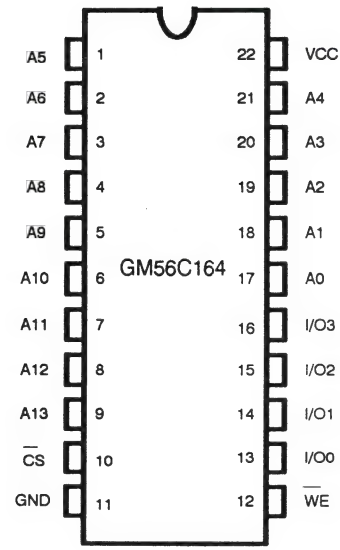
HIGH SPEED CMOS SRAM

Description

The GM56C164 is a high speed CMOS static RAM organized as 16384x4 bits. It is manufactured using GSS's high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 385mW.
The GM56C164 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60% when the circuit is deselected.
Easy memory expansion is provided by active low chip select ($\overline{CS}$) and three state dirvers.
All inputs and outputs of the GM56C164 are TTL compatible and operate from single 5V supply thus simplifying system design.
The GM56C164 is processed following the test methods of MIL STD 883C.

Pin Configuration

(Top View)



Features

- 16,384 x 4 organization
- High Speed.
  Fast Access and Cycle Time 25/35/45 ns (Max.)
- Low Power Standby and Low Power Operation
- Active : 267mW (Typ)
  Standby : 75mW (Typ)
- Completely Static Ram : No Clock or Timing Strobe Required
- Common I/O (Three-State Output)
- Directly TTL Compatible : All Inputs and Outputs
- Single +5V Operation (± 10%)
- Standard 22 DIP (300MIL)
- Capable of withstanding Greater than 2000V Electrostatic Discharge

Pin Name

$A_0 \sim A_{13}$	: Address Input
$\overline{WE}$	: Write Enable Input
$\overline{CS}$	: Chip Select Input
$I/O_0 \sim I/O_3$	: Data Input/Output
V_{CC}	: Power Supply, +5V
GND	: Ground

Absolute Maximum Ratings

Supply voltage to GND potential : -0.5V to + 7.0V
DC input voltage : -3.0V to +7.0V
DC output voltage in high Z state : -0.5V to 7.0V
Storage temperature : -65°C to + 150°C
Output Current into outputs (low) : 20mA
Electro static discharge voltage : >2000V (MIL STD 883C method 3015.2)

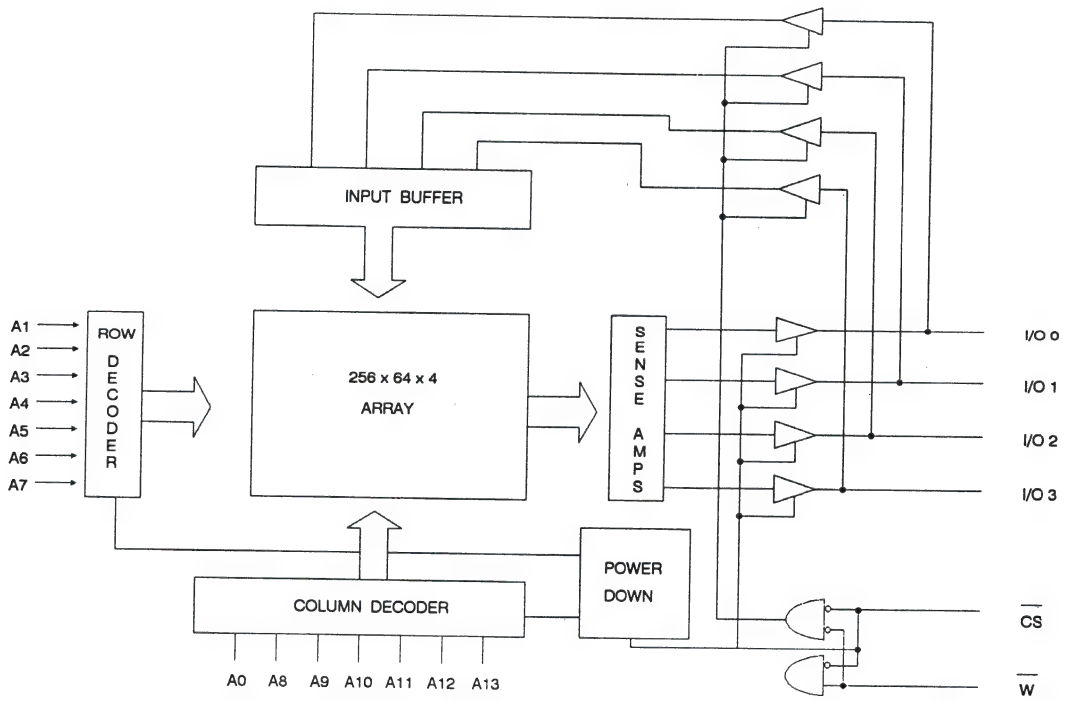
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions :

TA = 0°C to 70°C
VCC Supply Voltage 4.5V to 5.5V
VIH Input High Voltage 2.2 to VCC
VIL Input Low Voltage -3.0 to 0.8V
All voltages are referenced to GND pin = 0V

This device contains circuitry to protect the inputs against damage due to high static voltages or elec tric fields; however, it is advised that normal precau tions be taken to avoid application of any voltage hig her than maximum rated voltages to this high-impe dance circuit.

Function Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	MODE	I/O PIN	V_{CC} CURRENT	NOTE
H	X	Deselect	High Z	I_{SB}	
L	H	Read	Dout	I_{CC}	Read Cycle
L	L	Write	Din	I_{CC}	Write Cycle

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0° ~ 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP*	MAX	UNIT
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-10	-	+10	μA
I_{LO}	Output Leakage Current	CS = V_{IH}, $V_{I/O}$ = GND to V_{CC}	-10	-	+10	μA
I_{OS}*2	Output Short Circuit Current	V_{CC} = MAX, Vout = GND	-	-	-350	mA
I_{CC}	Average Operating Current	MIN. cycle, duty = 100%, $I_{I/O}$ = 0mA, V_{CC} = MAX. V_{IN} = V_{CC} or GND	-	-	70	mA
I_{SB}	Standby Power Supply Current	CS ≥ V_{IH}	-	-	30	mA
V_{OL}	Output Voltage	I_{OL} = 8.0mA	-	-	0.4	V
V_{OH}		I_{OH} = -4.0mA	2.4	-	-	V

* Typical limits are at V_{CC} = 5.0V, TA = 25°C and specified loading.

*2 Duration of the short circuit should not exceed 30 seconds.

Capacitance : (T_A = 25°C, f = 1MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_I = 0V	-	5	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	7	

Note : This parameter is sampled and not 100% tested,.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing References	1.5 V
Output Load (IOL/IOH)	Fig 1 & 2

including scope and jig.

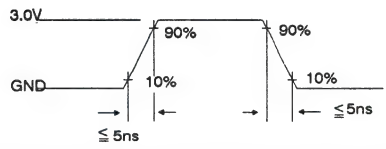


Figure 1 Output Load

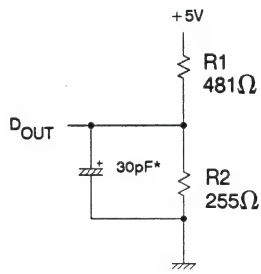
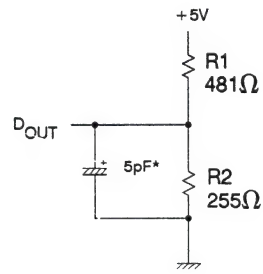


Figure 2 Output Load

(t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



AC Operating Characteristics: V_{CC} = 5V ± 10%, T_A = 0°C ~ 70°C

• Read Cycle

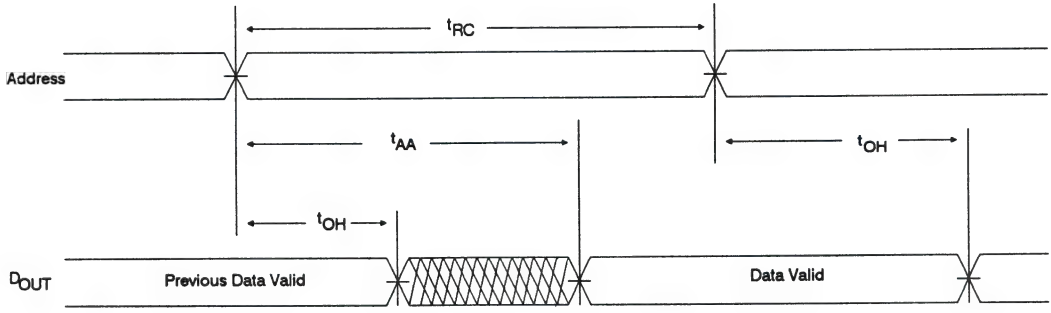
SYMBOL	PARAMETER		GM56C164-25		GM56C164-35		GM56C164-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time		25		35	_	45	_	ns
t_{AA}	Address Access Time		_	25	_	35	_	45	ns
t_{ACS}	Chip Select Access Time	$\overline{CS}$	_	25	_	35	_	45	ns
t_{LZ}	Chip Selection to Output in Low Z	$\overline{CS}$	3	_	3	_	3	_	ns
t_{HZ}	Chip Deselection to Output in High Z	$\overline{CS}$	0	10	0	15	0	15	ns
t_{OH}	Output Hold from Address Change		3	_	3	_	3	_	ns
t_{PU}	$\overline{CS}$ Low to Power Up		0	_	0	_	0	_	ns
t_{PD}	$\overline{CS}$ High to Power Down		_	25	_	35	_	45	ns

• Write Cycle

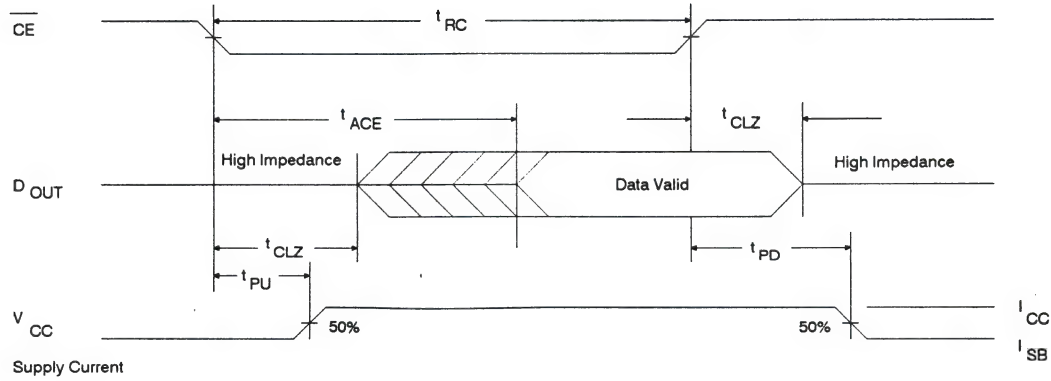
SYMBOL	PARAMETER	GM56C164-25		GM56C164-35		GM56C164-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	25	_	35	_	45	_	ns
t_{CW}	$\overline{CS}$ Low to Write End	20	_	30	_	35	_	ns
t_{AS}	Address Setup Time	0	_	0	_	0	_	ns
t_{AW}	Address Valid to End of Write	20	_	25	_	35	_	ns
t_{WP}	Write Pulse Width	20	_	25	_	35	_	ns
t_{WR}	Write Recovery Time (Address Hold from end of Write)	0	_	0	_	0	_	ns
t_{WZ}	Write to Output in High Z	_	7	_	10	_	15	ns
t_{DW}	Data Setup Time	13	_	15	_	20	_	ns
t_{DH}	Data Hold from Write Time	0	_	0	_	5	_	ns
t_{OW}	Output Active from End of Write	3	_	3	_	3	_	ns

Timing Waveforms

•READ CYCLE (1) : note (1, 2)

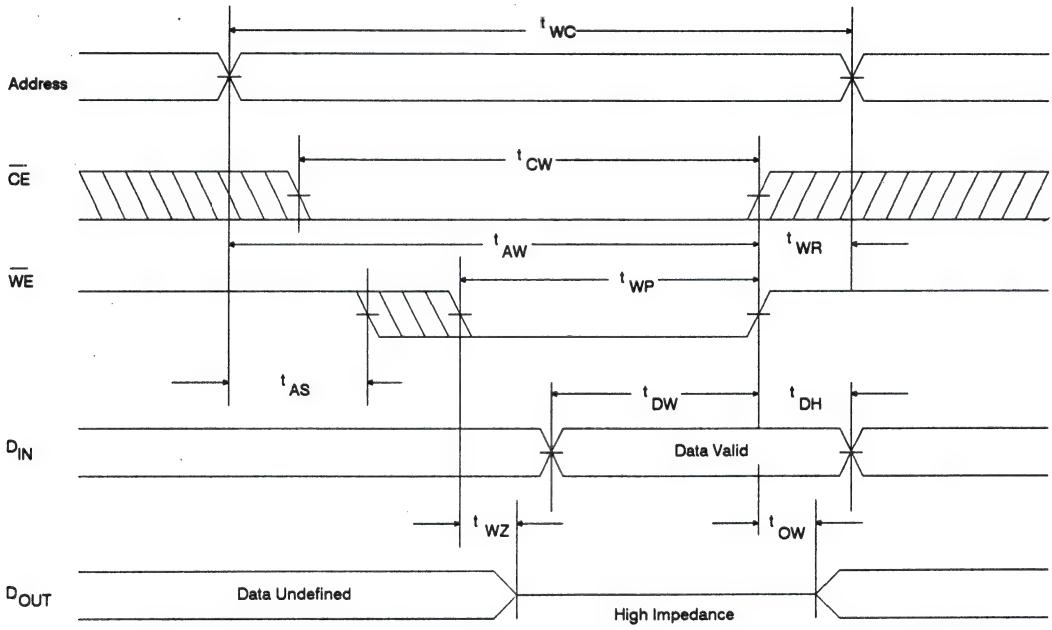


•READ CYCLE (2) : note (1, 3)

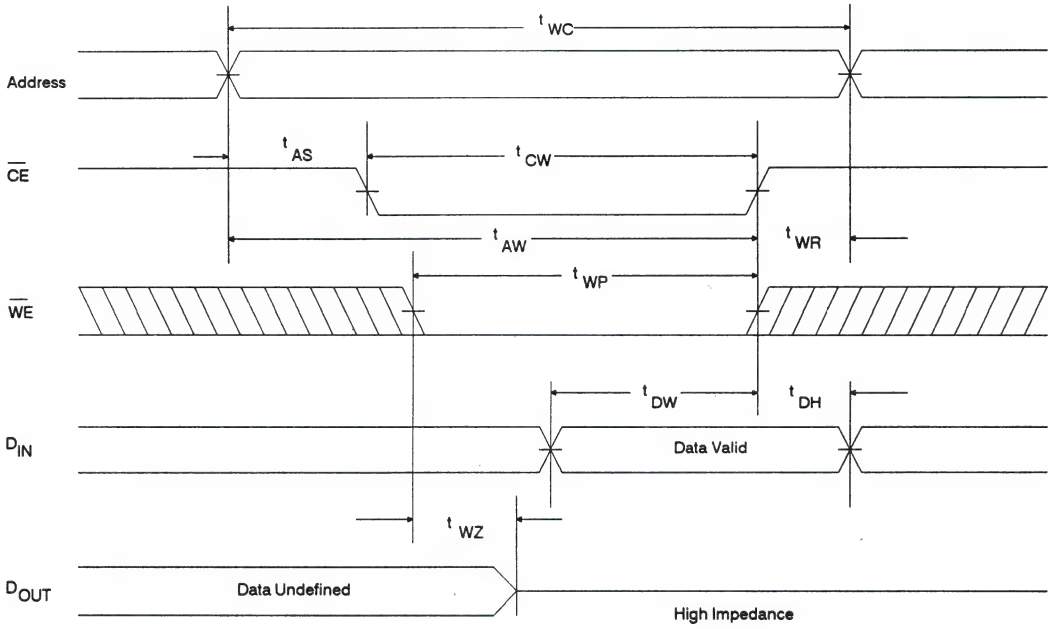


NOTE : 1 : $\overline{WE}$ is High for read cycle
2 : Device is continuously selected. $\overline{CS}$ = V_{IL}
3 : Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE (1) : $\overline{WE}$ Controlled



•WRITE CYCLE (2) : $\overline{CS}$ Controlled



NOTES: 1. A write occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
5. During the t_{WZ}. I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS}$ is low during the t_{DH} and t_{OW}, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

PRELIMINARY SPECIFICATION

GM76C256

32,768x8 BIT STATIC RAM HIGH PERFORMANCE

Description

The GM76C256/L is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a typical operating current of 80mW/MHz and minimum cycle time of 85ns.

When $\overline{CS}$ is a logical high, the device is placed in low power standby mode in which standby current is 2mA typically. The GM76C256 has two control inputs. Chip select ($\overline{CS}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the GM76C256 is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256/L is offered in 28 pin DIP(600mil) and SOP(330mil).

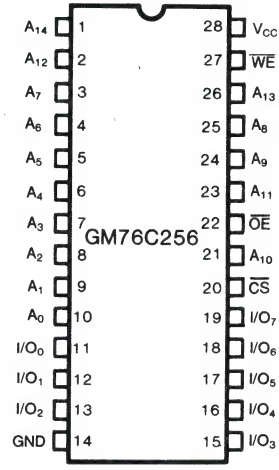
Feature

- **High Speed: Fast Access and Cycle Time 85/100/120/150 ns(Max.)**
- **Low Power Standby and Low Power Operation; Stand by : 0·55mW (Max) Operation: Operation: 385mW (Max)**
- **Completely Static RAM: No Clock or Timing Strobe Required**
- **Equal Access and Cycle Time**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Standard 28 DIP and SOP**
- **Capability of Battery Back up Operation**

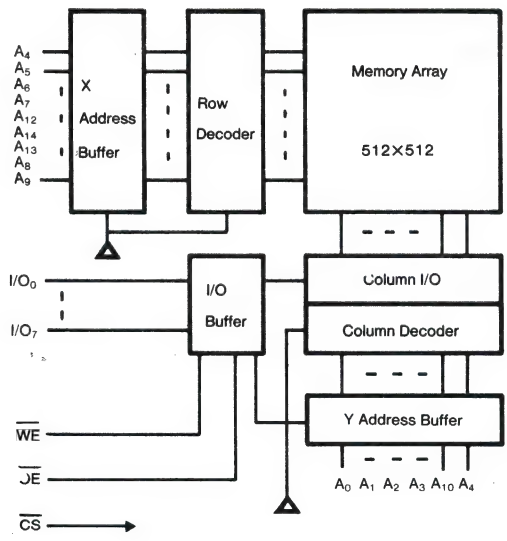
Pin Name

$A_0 \sim A_{14}$	:	Address Input
$\overline{WE}$	:	Write Enable Input
$\overline{OE}$	:	Output Enable Input
$\overline{CS}$	:	Chip Select Input
$I/O_0 \sim I/O_7$	:	Data Input/Output
V_{CC}	:	Power Supply, +5V
GND	:	Ground

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Input Voltage	V_{IN}	−0.3 to 7.0V
Supply Voltage	V_{CC}	−0.5 to 7.0V
Supply Voltage Applied to Outputs High Z State	V_{CC} (High Z)	−0.5 to 7.0V
Storage Temperature	T_{STG}	−65 to +150°C
Storage Temperature with Power Supplied	T_{power}	−55 to +125°C
Output Current Into Output	I_O	10mA

Recommended Operating Condition: T_A=0°∼70°C

Supply Voltage	V_{CC}	4.5 to 5.5V
Input High Voltage	V_{IH}	2.2 to 6V
Input Low Voltage	V_{IL}	−0.3 to 0.8V
Data Retention Supply Voltage	V_{DH}	2.0 to 5.5V

DC Electrical Characteristics: (V_{CC}=5V±10%, T_A =0°∼70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	GM76C256		UNITS
			MIN	MAX	
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=−1.0mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=2.1mA		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC}	V
V_{IL}	Input Low Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−2	2	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I V_{CC} Output Disabled	−2	2	μA
I_{SB}	Stand-by Power Supply Current	$\overline{CS}$=V_{IH}		20	mA
I_{SB1}		$\overline{CS}$=V_{CC}−0.2V		Note	μA
I_{CC}	Operating Supply Current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA		40	mA
I_{CC1}	Average Operating Power Supply Current	Min Cycle, duty=100% $I_{I/O}$=0 mA		70	mA

Note: GM76C256: 1mA, GM76C256L: 100 μA

AC Operating Characteristics: V_{CC}=5V±10%, T_A=0°∼70°C (Note 2)

- **Read Cycle**

SYMBOL	PARAMETER	GM76C256-85		GM76C256-10		GM76C256-12		GM76C256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycel Time	85	—	100	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	—	150	ns
t_{OE}	Output Enable to Output Valid	—	45	—	50	—	60	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	10	—	10	—	10	—	ns
t_{CLZ}	Chip Selection to Output in Low Z	10	—	10	—	10	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	30	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	0	40	0	50	ns

AC Operating Characteristics: V_{CC}=5V±10%, T_A=0°~70°C

- **Write Cycle**

SYMBOL	PARAMETER	GM76C256-85		GM76C256-10		GM76C256-12		GM76C256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	85	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	75	—	80	—	85	—	150		ns
t_{AW}	Address Valid to End of Write	75	—	80	—	85	—	100	—	ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	60	—	60	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write to Output in High Z	0	30	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	40	—	40	—	50	—	60		ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTES:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. AC operating conditions assume signal transition times of 5ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
3. t_{HZOE} and t_{HZCE} are tested with C_L=5 pF as in Figure 1b condition is measured ± 500 mV from steady state voltage.
4. By given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for all devices. These parameters are sampled and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data intput setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is high for read cycle.
7. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}
8. Address valid prior to or coincident with $\overline{CE}$ transition low.

Capacitance

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	T_A=25°C, f=1 MHz		6	pF
C_{OUT}	Output Capacitance	V_{CC}=5.0V		8	

Notes: Tested on a sample basis

AC Test Loads and Waveforms

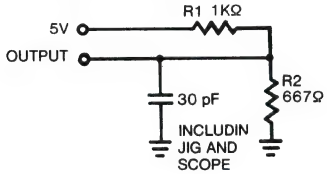


Figure 1a

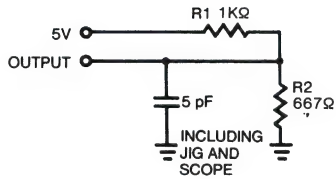


Figure 1b

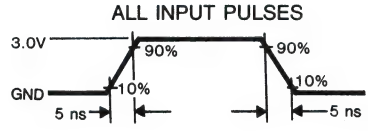
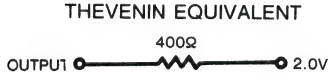
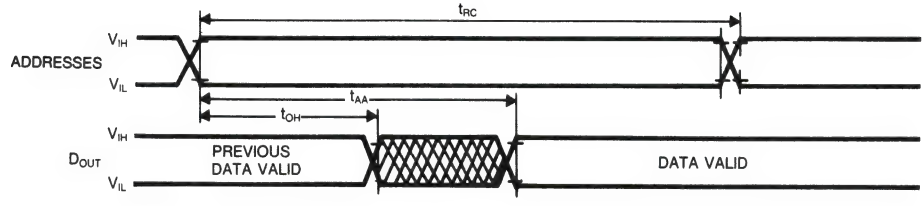


Figure 2

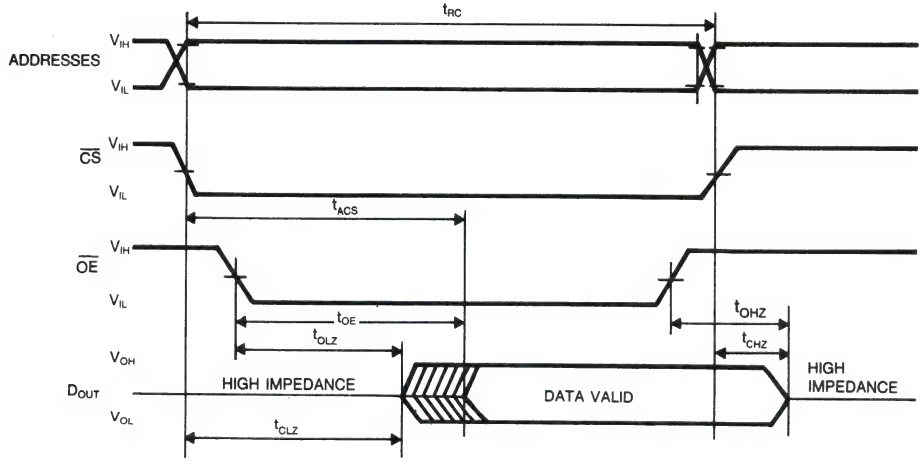


Timing Waveforms

Read Cycle 1 (Notes 6,7)

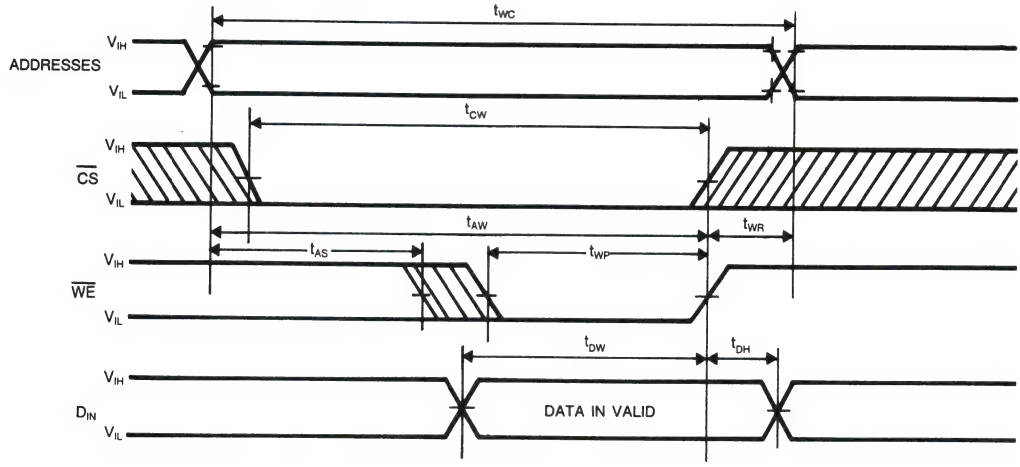


Read Cycle 2 (Notes 6,8)

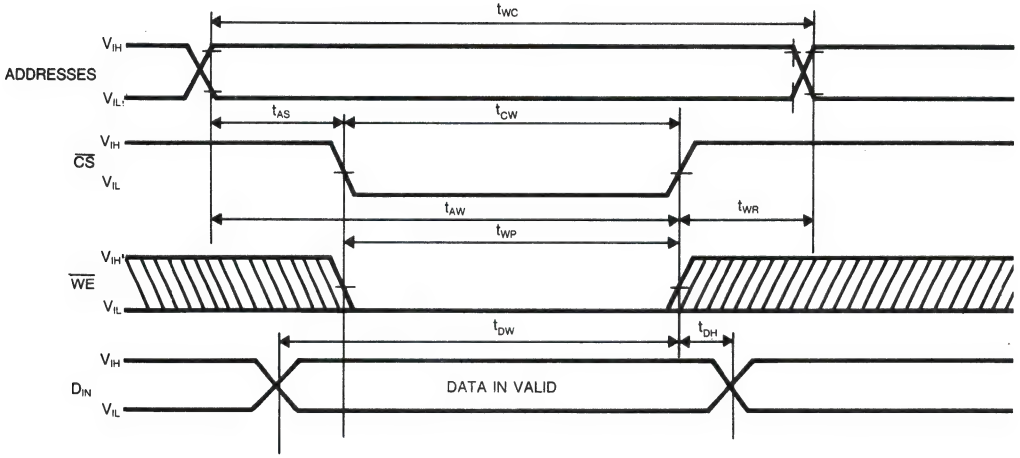


Timing Waveforms

Write Cycle 1 ($\overline{WE}$ Controlled) (Note 5)



Write Cycle 2 ($\overline{CS}$ Controlled) (Note 5)



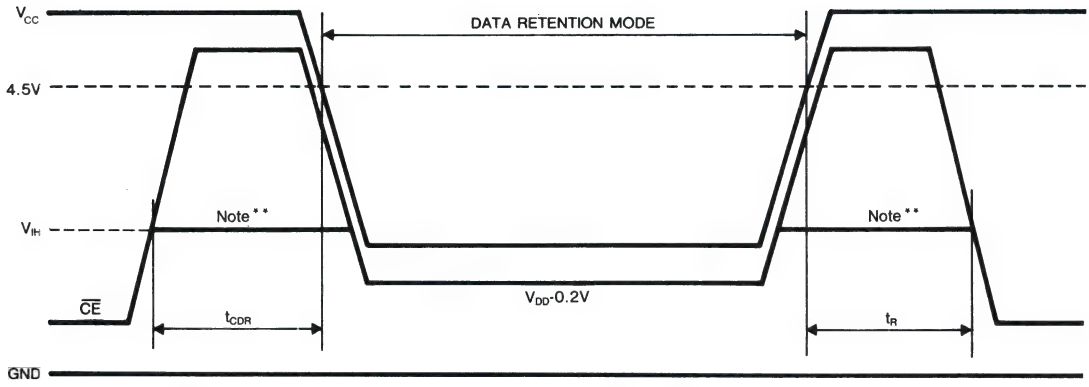
Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ High, the output remains in a high impedance state.

Data Retention Characteristics: (T_A=0°~70°C)

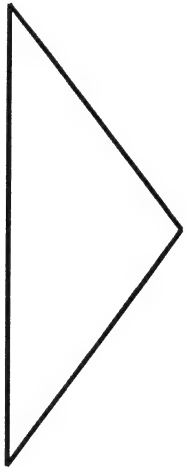
SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{DH}	Data Retention Supply Voltage	2.0	5.5	V	$\overline{CS} \geq V_{CC}-0.2V$
I_{DDS2}	Data Retention Current	—	50	μA	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$
t_{CDR}	Chip Deselection to Data Retention Mode	0	—	ns	
t_R	Recovery Time	t_{RC}	—	ns	

Note*: Read Cycle Time

$\overline{CE}$ Controlled Data Retention Mode



Note **: If the V_{IH} of $\overline{CS}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{CC} voltage is going down from 4.5V to 2.2V



PRODUCT SPECIFICATION

GM71256

262,144 x 1BIT DYNAMIC RAM

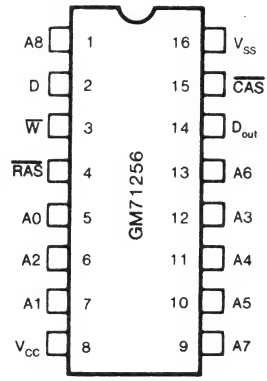
Description

The GM71256 is high speed, high performance dynamic RAM,organized 262,144 and manufactured using advanced NMOS silicon-gate technology. The design is optimised for both high speed and low power dissipation.

The GM71256 features multiplexed addressing, and all input signals, include clocks, are TTL-compatible, input and output signals are the same polarity, and the 3-state output buffer is $\overline{CAS}$ controlled. The Hi-C single transistor memory cell is used to enhance signal margin and reduce the α particle included soft error. This device offers page mode operation which allows high speed random access memory cells within the same row.

The GM71256 features single power supply of 5V±10% tolerance and is available a 16 pin plastic DIP or cerdip

Pin Configuration



Features

- **262,144 words x 1-bit organization**
- **100/120/150 ns access time from $\overline{RAS}$**
- **50/60/75 ns access time from $\overline{CAS}$**
- **385/360/330 mW active power, Page Mode,**
- **25 mW standby power**
- **Multiplexed address inputs**
- **±10% power supply tolerance**
- **Read-Modify-Write capabilities**
- **$\overline{RAS}$ Only Refresh/Hidden Refresh**
- **Latched or high impedance output during refresh**
- **256 refresh cycles/4ms**
- **Page Mode operation**

Pin Description

V_{CC}	+5V Supply
D	Data In
D_{out}	Data Out
A_0-A_8	Address Input (0-8)
$\overline{W}$	Write Enable
$\overline{RAS}$	Row Enable
$\overline{CAS}$	Column Enable
V_{SS}	Ground
NC	No Connect

Absolute Maximum Ratings*

PARAMETER	SYMBOL	VALUE	UNIT
Voltage Range on V_{CC} Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	PD	1.0	W
Case Operating Temperature Range	T_C	0 to 85	°C
Ambient Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range**	T_{stg}		
Ceramic Package		−65 to +160	°C
Plastic Package		−55 to +120	°C
Short Circuit Output Current	I_{OS}	50	mA

* Maximum Ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result. Extended operation at any of these conditions may result in reduced reliability.

** Bonding or soldering of the external pins of these devices can be performed safely at temperatures up to 300°C.

Recommended Opreating Conditions: (T_A=0 to 70°C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltages	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input Voltages* High Level—All Inputs (Logic 1) Low Level—All Inputs (Logic 0)	 V_{IH} V_{IL}	 2.4 −1.0	 — —	 6.5 0.8	 V V
Refresh Cycle Time**	t_{REF}	—	—	4.0	ms

* Application of invalid levels may destroy stored information during that cycle as well as the first cycle using valid levels. Data out is indeterminate.

** Addresses A0-A7 are used for refresh. A8 must be a valid one or zero.

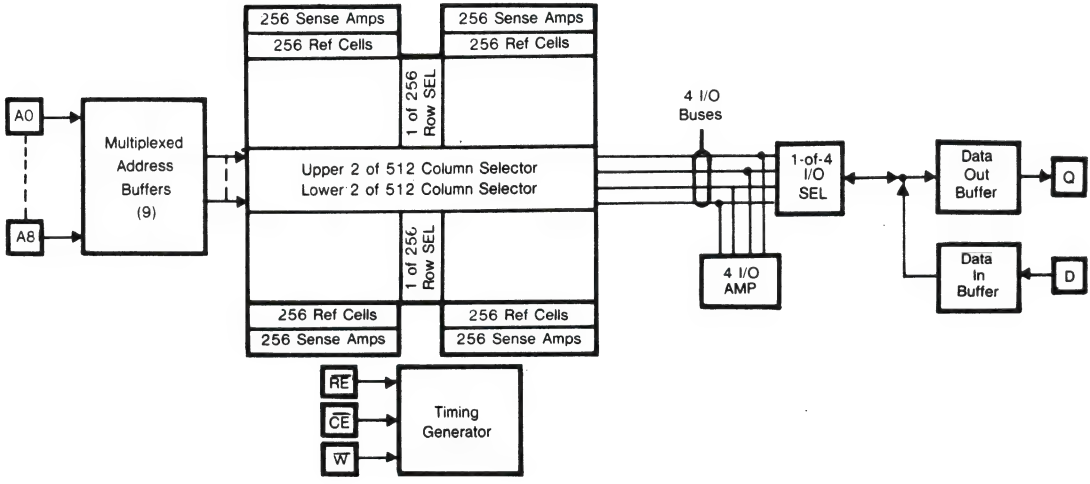


Figure 1. GM71256 Dynamic RAM Block Diagram

Electrical Characteristics: (V_{CC}=5V ±10%, V_{SS}=0V, T_A=0 to 70°C)

PARAMETER	SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Output Voltages								
Low Level (I_{OL}=4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
High Level (I_{OH}=−5.0mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
Power Supply Currents Operating Current (Average Operating Current $\overline{RAS}$ & $\overline{CAS}$ Cycling, t_{RC}=minimum)	I_{CC1}	—	70*	—	65*	—	60*	mA
Standby Current ($\overline{RAS}$=V_{IH}, Q=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
Refresh Current (Average Operating Current, Refresh Mode Operation) $\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, t_{RC}=min.	I_{CC3}	—	55*	—	50*	—	45*	mA
Page Mode Current (Average Operating Current, Page Mode Operation, $\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling, t_{PC}=minimum)	I_{CC4}	—	50*	—	45*	—	40*	mA
Input Leakage Current (V_{CC}=5.5 V, V_I=0 to 6.5 V, All other leads at 0 V)	I_I	−10	10	−10	10	−10	10	μA
Output Leakage Current (Q=High Impedance, V_Q=0 to V_{CC})	I_O	−10	10	−10	10	−10	10	μA
Input Capacitance (A0-A8)**	C_{11}	—	5	—	5	—	5	pF
Input Capacitance (D, $\overline{W}$ Leads)**	C_{12}	—	5	—	5	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$ Leads)**	C_{13}	—	10	—	10	—	10	pF
Output Capacitance (Q Lead)**	C_O	—	7	—	7	—	7	pF

* Maximum occurs at T_A=0°C, I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} are specified with output open-circuited.
** Parameter periodically sampled and not 100% tested.

Timing Characteristics: (V_{CC}=5V ±10%, V_{SS}=0V, T_A=0 to 70°C) (Notes 1, 2, and 3)

DESCRIPTION	SYMBOL	JEDEC SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Random Read/Write Cycle Time	t_{RC}	t_{RELREL}	200	—	220	—	260	—	ns
Access Time from $\overline{RAS}$ (Notes 4 & 5)	t_{RAC}	t_{RELQV}	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$ (Notes 5 & 6)	t_{CAC}	t_{CELQV}	—	50	—	60	—	75	ns
Output Buffer Time Off Delay (Note 7)	t_{OFF}	t_{CEHQZ}	0	20	0	30	0	30	ns
Transition Time	t_T	t_T	2	50	2	50	2	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	t_{REHREL}	90	—	90	—	100	—	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	t_{RELREH}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	t_{CELREH}	50	—	60	—	75	—	ns
$\overline{CAS}$ Pulse Width (Note 8)	t_{CAS}	t_{CELCEH}	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	t_{RELCEH}	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay (Note 4)	t_{RCD}	t_{RELCEL}	25	50	25	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	t_{CEHREL}	0	—	0	—	0	—	ns
Row Address Setup Time	t_{ASR}	t_{RAVREL}	0	—	0	—	0	—	ns
Row Address Hold Time	t_{RAH}	t_{RELRAX}	15	—	15	—	15	—	ns
Column Address Setup Time	t_{ASC}	t_{CAVCEL}	0	—	0	—	0	—	ns
Column Address Hold Time	t_{CAH}	t_{CELCAX}	20	—	25	—	30	—	ns
Column Address Hold Time Ref. to $\overline{RAS}$	t_{AR}	t_{RELCAX}	75	—	90	—	105	—	ns
Read Command Hold Time Ref. to $\overline{RAS}$	t_{RRH}	t_{REHWX}	10	—	10	—	10	—	ns
Read Command Setup Time	t_{RCS}	t_{WHCEL}	0	—	0	—	0	—	ns
Read Command Hold Time Ref. to $\overline{CAS}$	t_{RCH}	t_{CEHWX}	0	—	0	—	0	—	ns
Write Command Hold Time	t_{WCH}	t_{CELWX}	15	—	20	—	25	—	ns
Write Command Hold Time Ref. to $\overline{RAS}$	t_{WCR}	t_{RELWX}	85	—	100	—	120	—	ns
Write Command Pulse Width	t_{WP}	t_{WLWH}	15	—	20	—	25	—	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	t_{WLREH}	30	—	35	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	t_{WLCEH}	20	—	30	—	40	—	ns
Data In Setup Time	t_{DS}	t_{DVCEL}	0	—	0	—	0	—	ns
Data In Hold Time	t_{DH}	t_{CELDX}	15	—	20	—	25	—	ns
Data In Hold Time Ref. to $\overline{RAS}$	t_{DHR}	t_{RELDX}	85	—	100	—	120	—	ns
Write Command Setup Time (Note 9)	t_{WCS}	t_{WLCEL}	0	—	0	—	0	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay (Read-Modify-Write)	t_{CWD}	t_{CELWL}	25	—	30	—	35	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay (Read-Modify-Write) (Note 6)	t_{RWD}	t_{RELWL}	75	—	100	—	125	—	ns
Data In Hold Time (Read-Modify-Write) (Note 6)	t_{DH}	t_{WLDX}	20	—	20	—	20	—	ns
Data In Setup Time (Read-Modify-Write)	t_{DS}	t_{DVWL}	0	—	0	—	0	—	ns
Refresh Period	t_{REF}	t_R	—	4.0	—	4.0	—	4.0	ms
Cycle Time (Read-Modify-Write)	t_{RMW}	$t_{WRELREL}$	245	—	260	—	310	—	ns

DESCRIPTION	SYMBOL	JEDEC SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
PAGE MODE OPTION									
Page Mode Cycle Time	t_{PC}	t_{CELCEL}	120	—	130	—	145	—	ns
$\overline{CAS}$ Precharge Time	t_{CP}	t_{CEHCEL}	45	—	50	—	60	—	ns

Notes:

1. Timing specifications given assume t_T = 5ns.
2. V_{IH} (min), V_{IL} (max) are reference levels for timing specifications or inputs signals. Transition times are to be measured between these reference levels.
3. An initial pause of 100 μs followed by a minimum of 8 refresh cycles is necessary after V_{CC} is applied, to achieve proper device operation. Address A0-A7 are used for refresh. A8 must be a valid one or zero.
4. For $t_{RELCEL} > t_{RELCEL}$ (max.), t_{RELQV} will increase by the amount that t_{RELCEL} (max.) is exceded.
5. Q load assumed to be equivalent to 2 TTL loads and 100 pF.
6. Assumes $t_{RELCEL} \geq t_{RELCEL}$ (max.)
7. t_{CEHOZ} (max.) defines the time at which Q achieves the open circuit condition.
8. $\overline{CAS}$ can be held at Logic 0 for an indefinite time for latched output during refresh. However, t_{RELRAX} must be increased to 100ns.
9. Non-restrictive operating parameter. If $t_{WLCEL} \geq t_{WLCEL}$ (min.), the cycle is an early write cycle and the dat out (Q) will remain an open circuit (high impedance) for the entire cycle. If $t_{CELWL} \geq t_{CELWL}$ (min.) and $t_{RELWL} \geq t_{RELWL}$ (min.), the cycle is a read-write cycle and the data out (Q) will validly reproduce the data contained in the selected cell. If neither of the above sets or conditions is satisfied, data out will be indeterminate.

Timing Waveforms

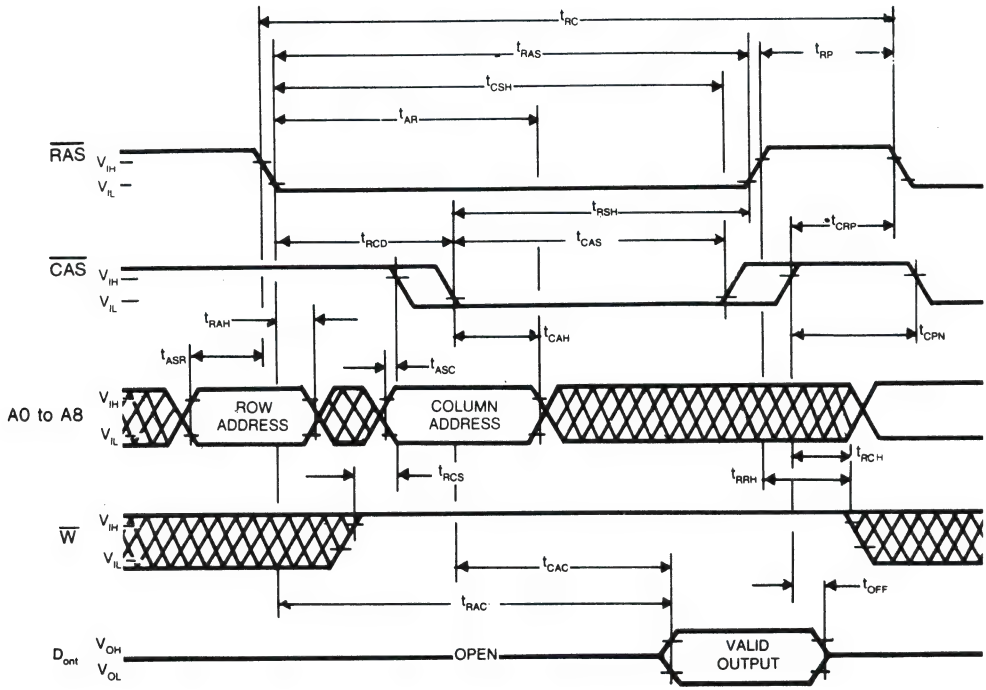


Figure 2 Read Cycle

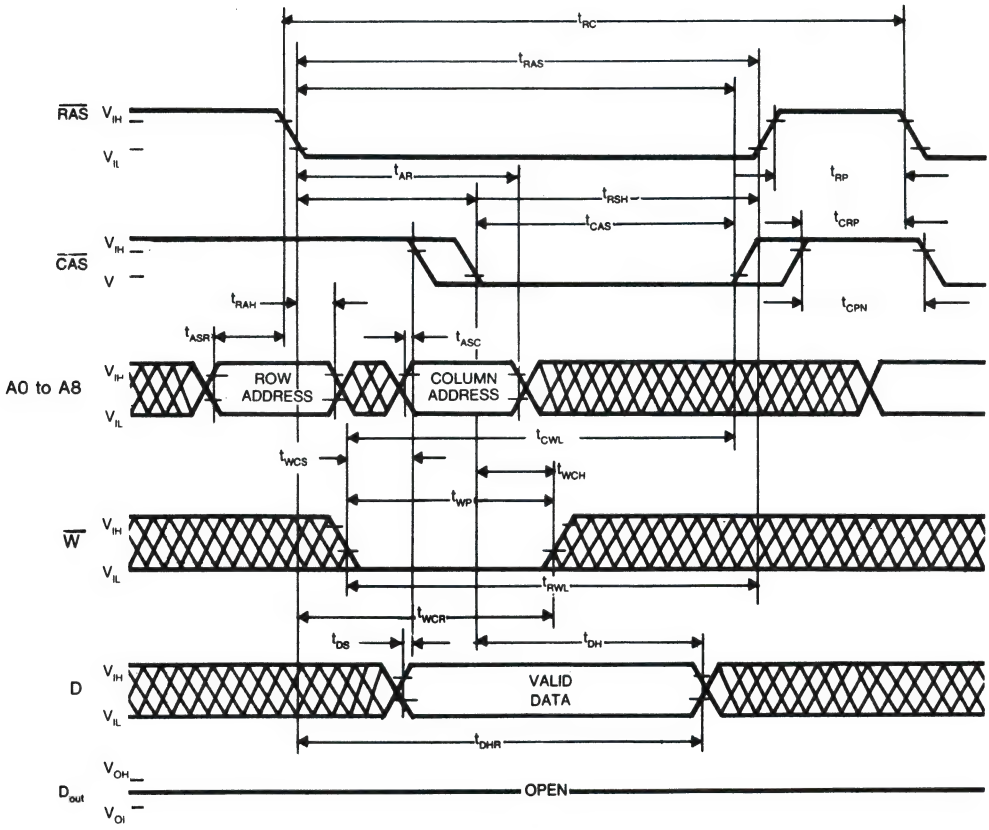


Figure 3. Write Cycle (Early Write)

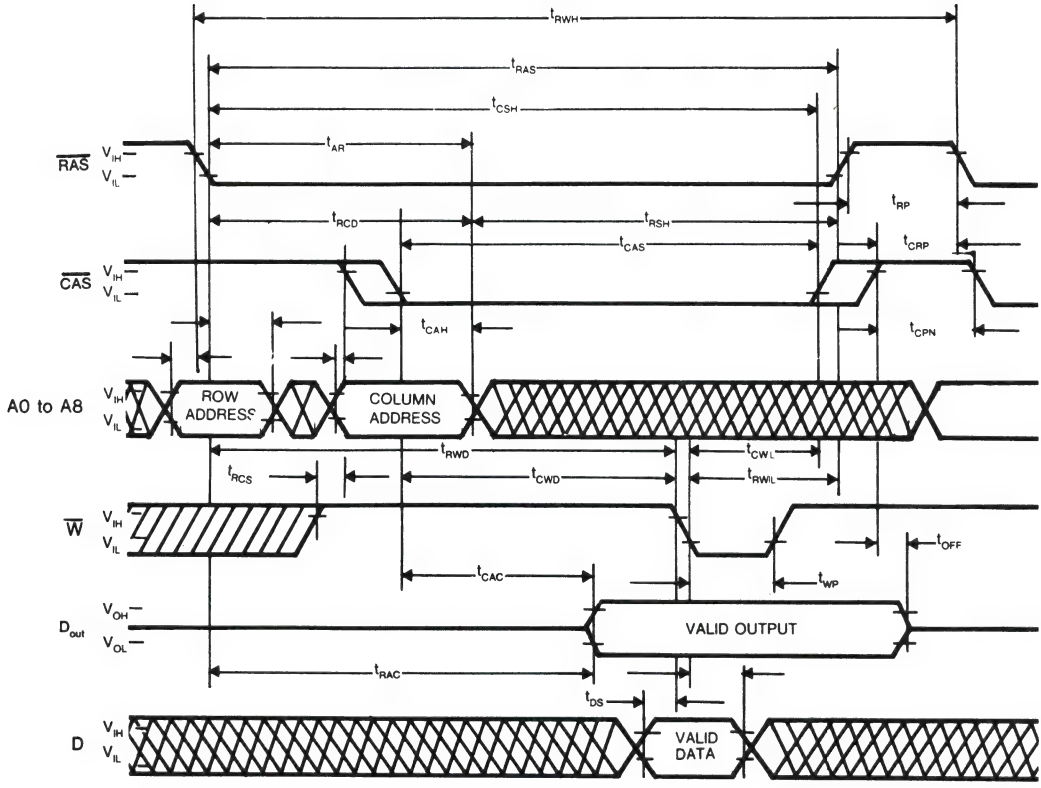
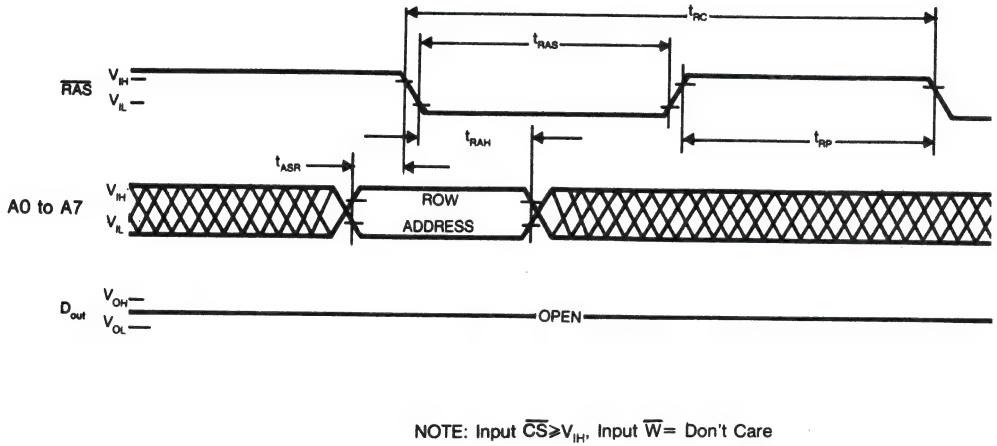


Figure 4. Read-Write/Read-Modify-Write Cycle



NOTE: Input $\overline{CS} \geq V_{IH}$, Input $\overline{W}$= Don't Care

Figure 5. $\overline{RAS}$ Only Refresh Cycle (Note 3)

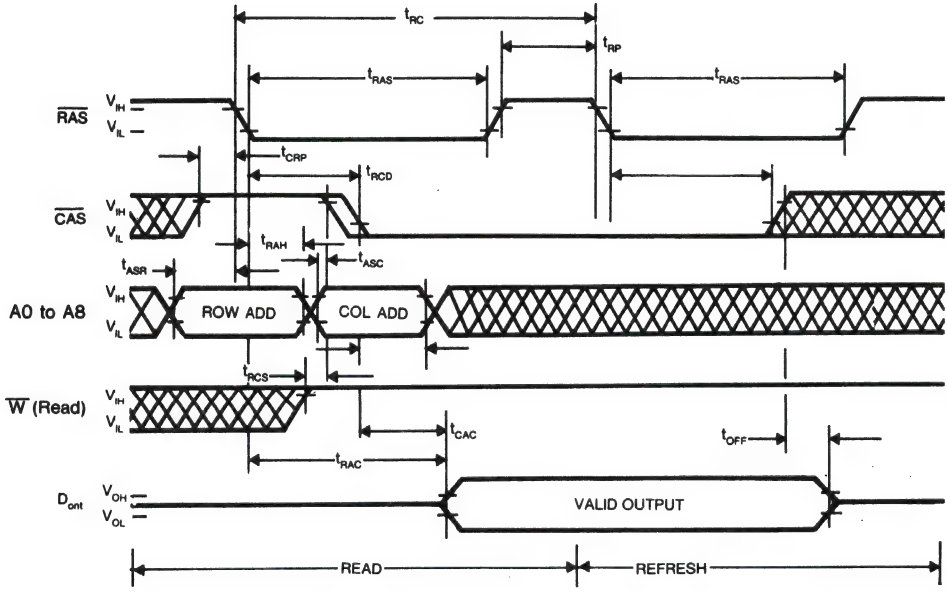


Figure 6. Hidden Refresh Cycle (Notes 3 and 8)

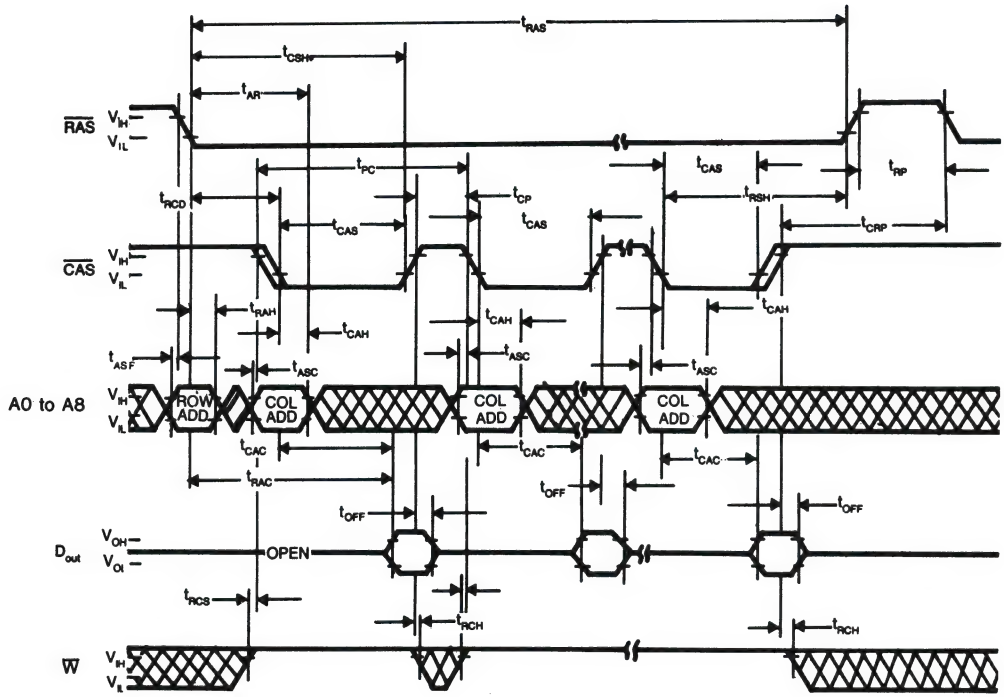


Figure 7. Page Mode Read Cycle

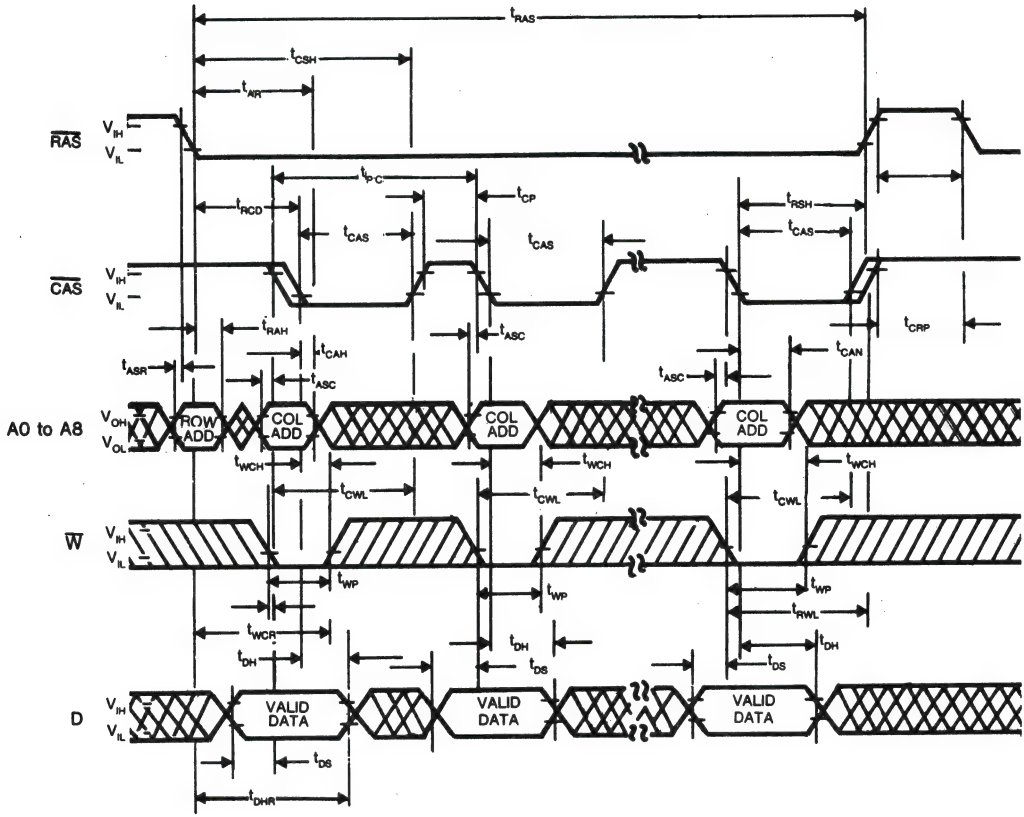


Figure 8. Page Mode Write Cycle

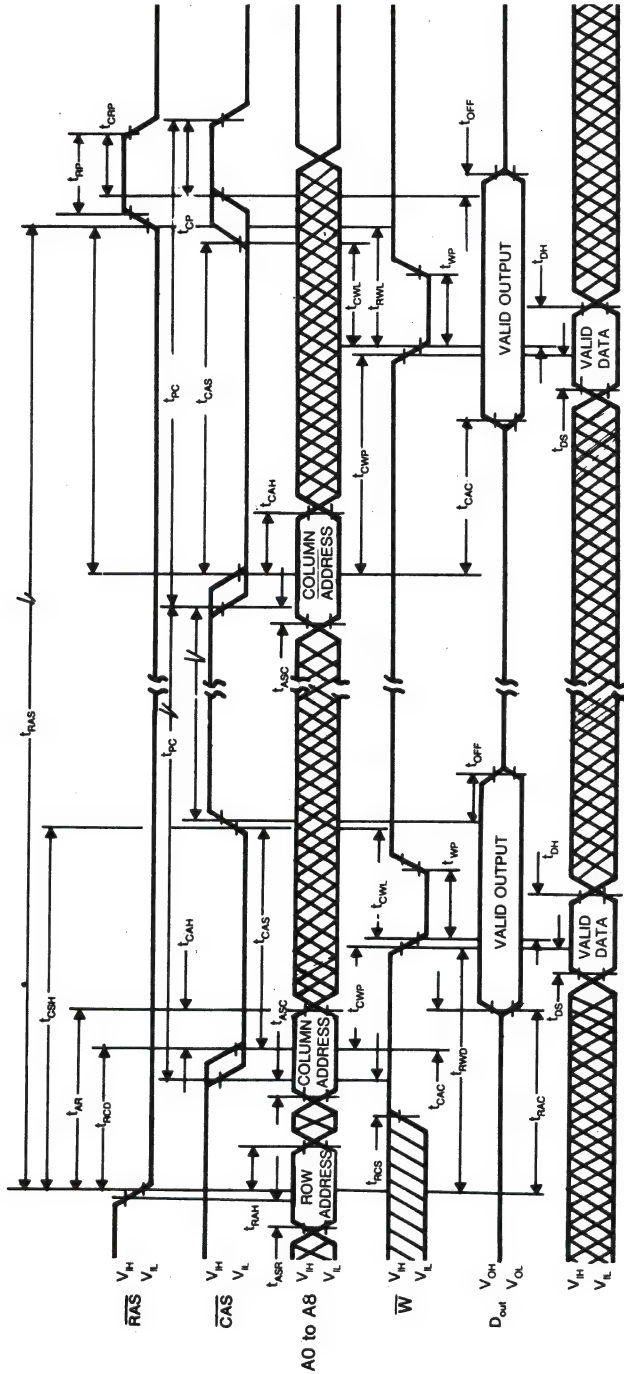


Figure 9. Page Mode Read-Modify-Write Cycle

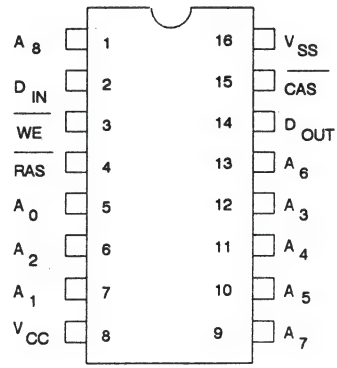
GM71C256
256K X 1 BIT CMOS DYNAMIC RAM

Description

The GM71C256 is a high speed dynamic RAM organized 262,144x1 Bit. The GM71C256 utilizes Goldstar's silicon Gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The GM71C256 offers Fast Page Mode which allows high speed random access memory cells within the same row. Multiplexed address inputs permit the GM71C256 to be packaged in a standard 16 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The GM71C256 is ideal for high speed, high performance systems such as mainfraim, minicomputer, graphics, PC and high performance μ-processor systems.

Pin Configuration

16 Plastic DIP



Features

- 262,144x1 Bit organization
- Fast access time and cycle time : 80/100/120 ns(Max)
- Single Power Supply of 5V ±10% with a built-in V_{BB} generator
- Performance Range

PARAMETER		GM71C256(ns)		
		-80	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	80	100	120
t_{AA}	Column Address Access Time	40	45	55
t_{CAC}	$\overline{CAS}$ Access Time	20	25	30
t_{RC}	Cycle Time	145	175	205
t_{PC}	Fast Page Mode Cycle Time	55	60	70

- Low Power
- 330mW MAX. Operating (GM71C256-80)
- 247mW MAX. Operating (GM71C256-12)
- 16.5mW MAX. Standby
- Read-Modify-Write, $\overline{RAS}$-only refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh and Fast Page Mode Capability
- All input and output TTL compatible
- 256 refresh cycles/4ms
- Industry standard 16 pin Plastic DIP.

Pin Description

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	+5V Supply
V_{SS}	0V Supply

Ordering Information

Type NO.	Access Time	PKG
GM71C256-80 GM71C256-10 GM71C256-12	80 ns 100 ns 120 ns	300 MIL 16 PIN PLASTIC DIP

Recommended Operating Conditions

(T_A = 0°C to 70°C)

V_{CC} Supply Voltage	4.5 ~ 5.5V
V_{IH} Input High Voltage	2.4 ~ 6.5V
V_{IL} Input Low Voltage	-1.0 ~ 0.8V

Absolute Maximum Ratings*

Ambient Temperature Under-Bias	0°C to +70°C
Storage Temperature (plastic)	-55°C to +125°C
Votage on any Pin Except V_{CC} Relative to V_{SS}	-1.0V to 7.0V
Voltage on V_{CC} relative to V_{SS}	-1.0V to +7.0V
Data Output Current	50mA
Power Dissipation	1.0W

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	–	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN)	80 100 120	-	60 50 45	mA	3, 4
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		-	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN)	80 100 120	-	60 50 45	mA	3
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN)	80 100 120	-	40 35 30	mA	3, 4
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		-	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	80 10 12		40 35 30	mA	
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	80 10 12		4 4 4	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 6.5V, All other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 6.5V)		-10	10	µA	

Capacitance (V_{CC} = 5V ±10%, f = 1MHz, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 - A8)	-	4	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	5	pF
C_O	Output Capacitance (D_{OUT})	-	6	pF

* Note : Capacitance is sampled and not 100% tested.

Electrical Characteristics And Recommended AC Operating Conditions

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C256-80		GM71C256-10		GM71C256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	145	-	175	-	205	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	60	-	70	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	110	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	-	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	-	30	ns	8, 13
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	55	-	65	ns	8, 14
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	55	-	65	-	75	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	75000	100	75000	120	75000	ns	
t_{RSH}(R)	$\overline{RAS}$ Hold Time (Read Cycle)	20	-	25	-	30	-	ns	
t_{RSH}(W)	$\overline{RAS}$ Hold Time (Write Cycle)	25	-	30	-	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	120	-	ns	
t_{CAS}(R)	$\overline{CAS}$ Pulse width in Read Cycle	20	75000	25	75000	30	75000	ns	
t_{CAS}(W)	$\overline{CAS}$ Pulse Width in Write Cycle	25	-	30	-	35	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	30	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	25	65	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	20	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	25	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	45	-	55	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	5	-	5	-	5	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5	-	5	-	ns	10
t_{AR}	Column Address Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{WCR}	Write Commend Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	60	-	70	-	80	-	ns	

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) Unit : nS (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C256-80		GM71C256-10		GM71C256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	15	-	20	-	25	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	20	-	25	-	ns	11
t_{REF}	Refresh Period (256 cycle)	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to Write Delay Time	20	-	25	-	30	-	ns	12
t_{RWD}	$\overline{RAS}$ to Write Delay Time (RMW)	80	-	100	-	120	-	ns	12
t_{AWD}	Column Address to Write Delay	40	-	45	-	55	-	ns	12
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CSR}	$\overline{CAS}$ Set Up Time $\overline{CBR}$ Refresh	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ Before $\overline{RAS}$ Refresh	25	-	30	-	40	-	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	-	25	-	30	-	ns	
t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse width	110	-	135	-	160	-	ns	

Notes

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltage are refrenced to V_{SS}
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μS is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5nS.
7. V_{IH} (min) and V_{IL} (max) are referenced levels for measuring timing of input signals. Also transition times are required between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves the open circuit condition and is not refrenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle: If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min) the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a referenced point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by tCAC.
14. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a referenced point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by tAA.

Timing Waveforms

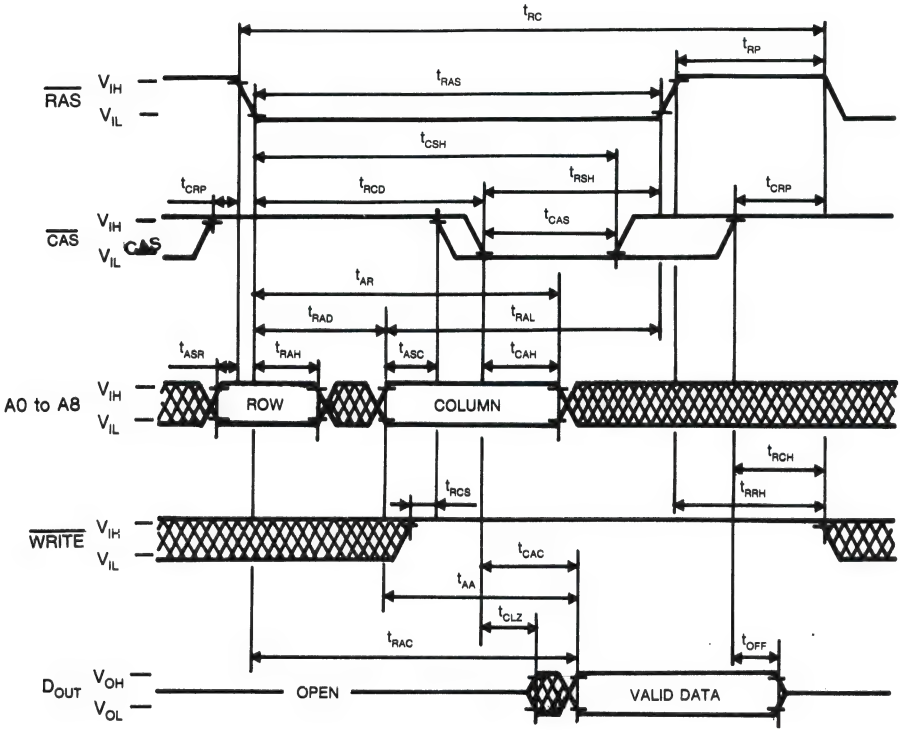


Figure 2 Read Cycle

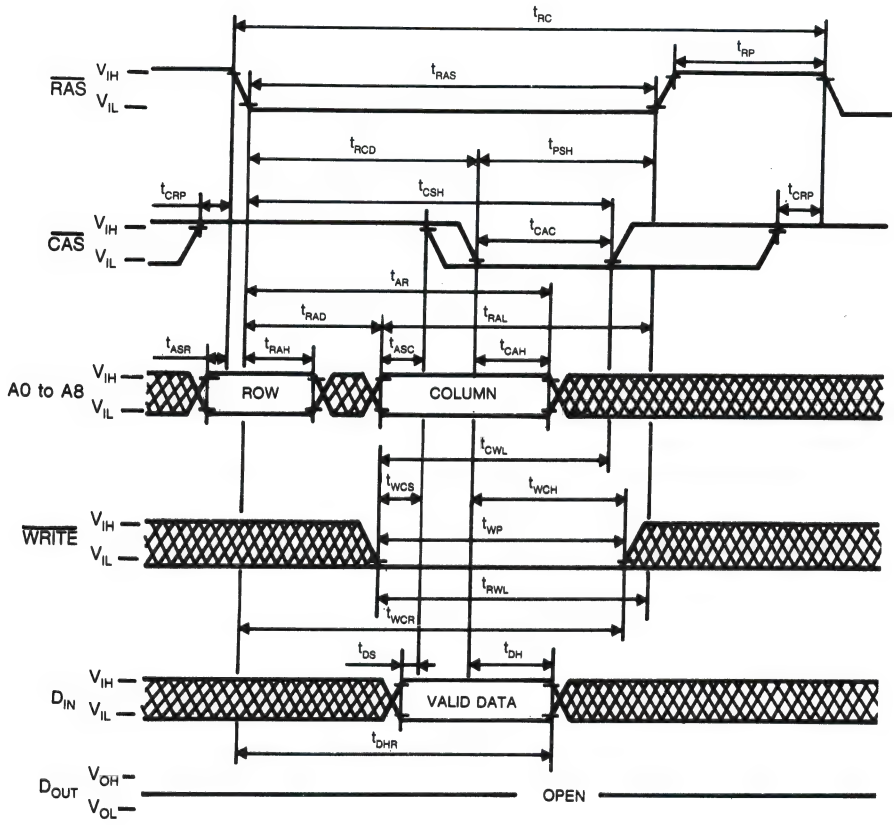


Figure 3 Write Cycle

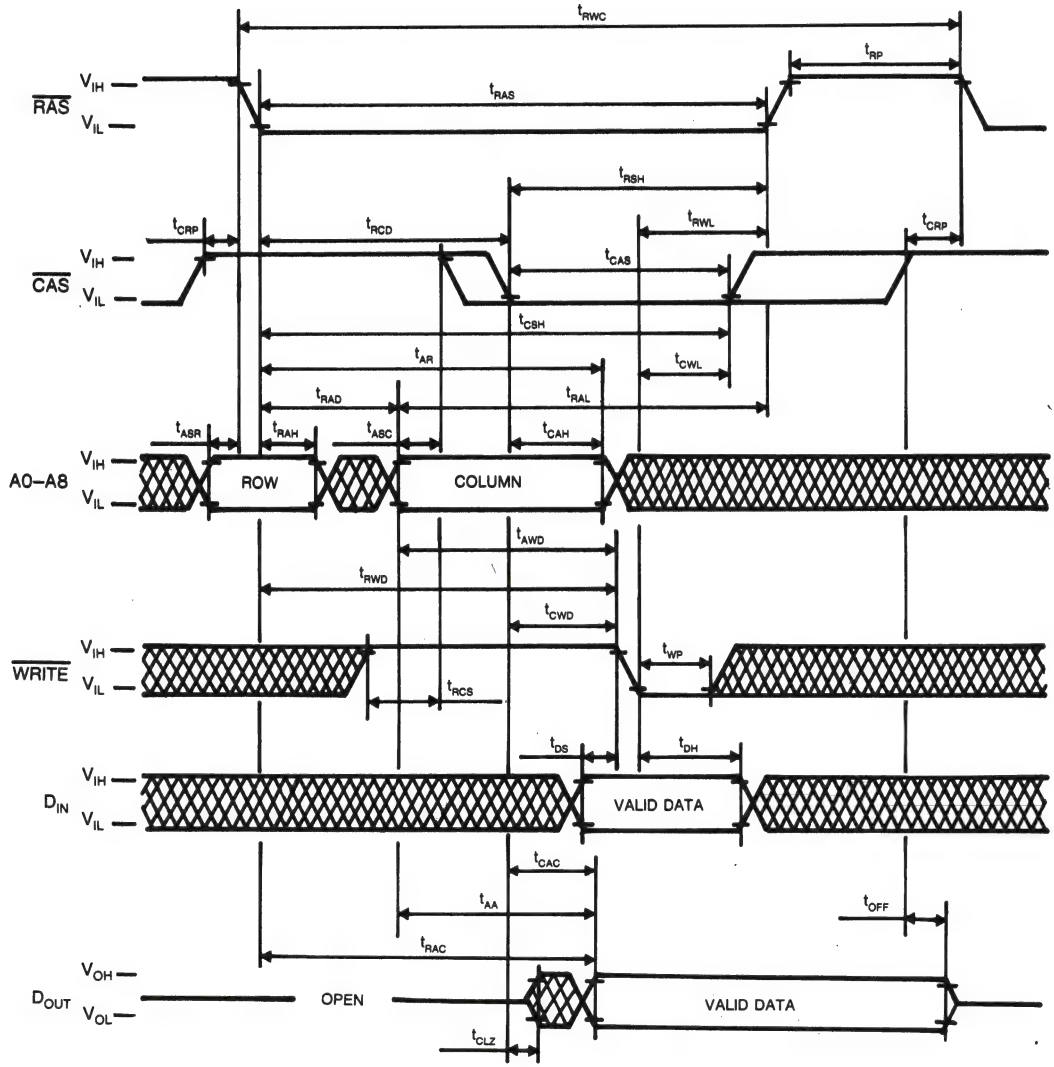


Figure 4. Read-Write Cycle

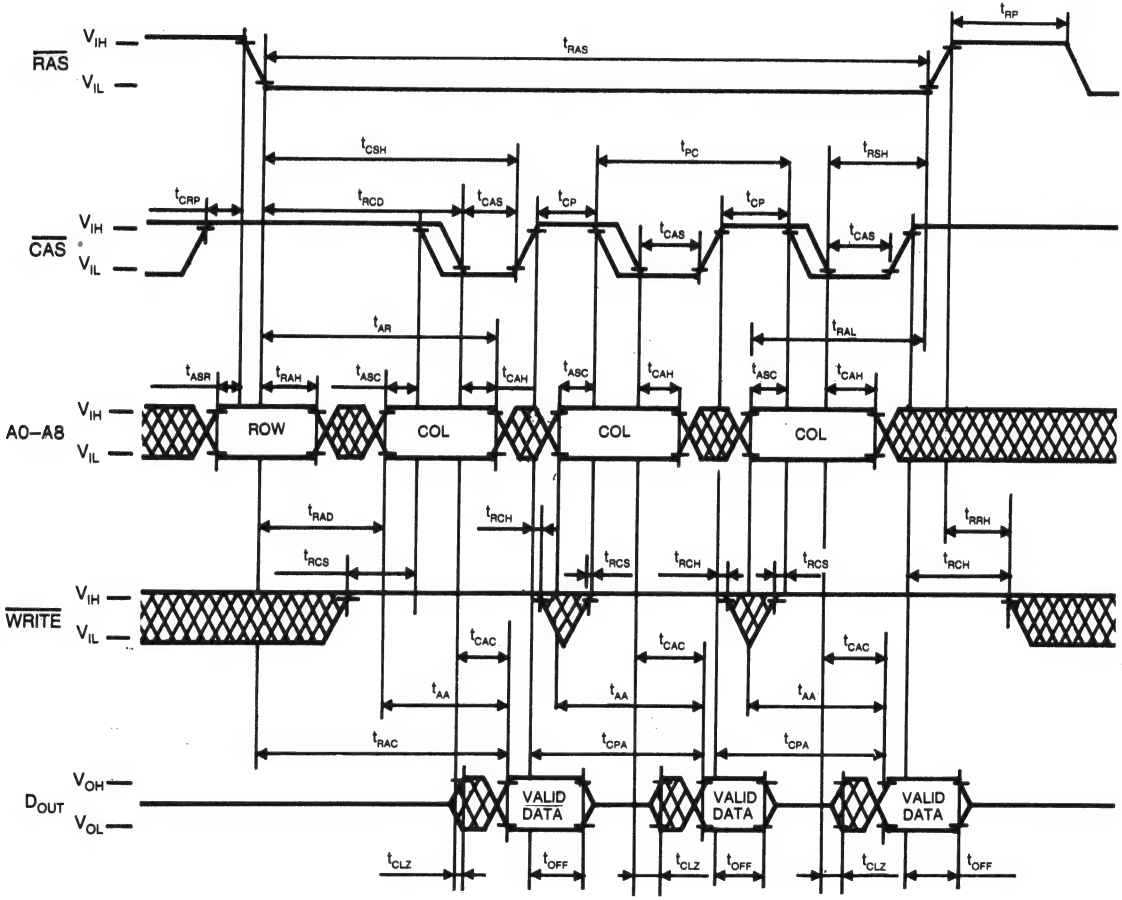


Figure 5. Fast Page Mode Read Cycle

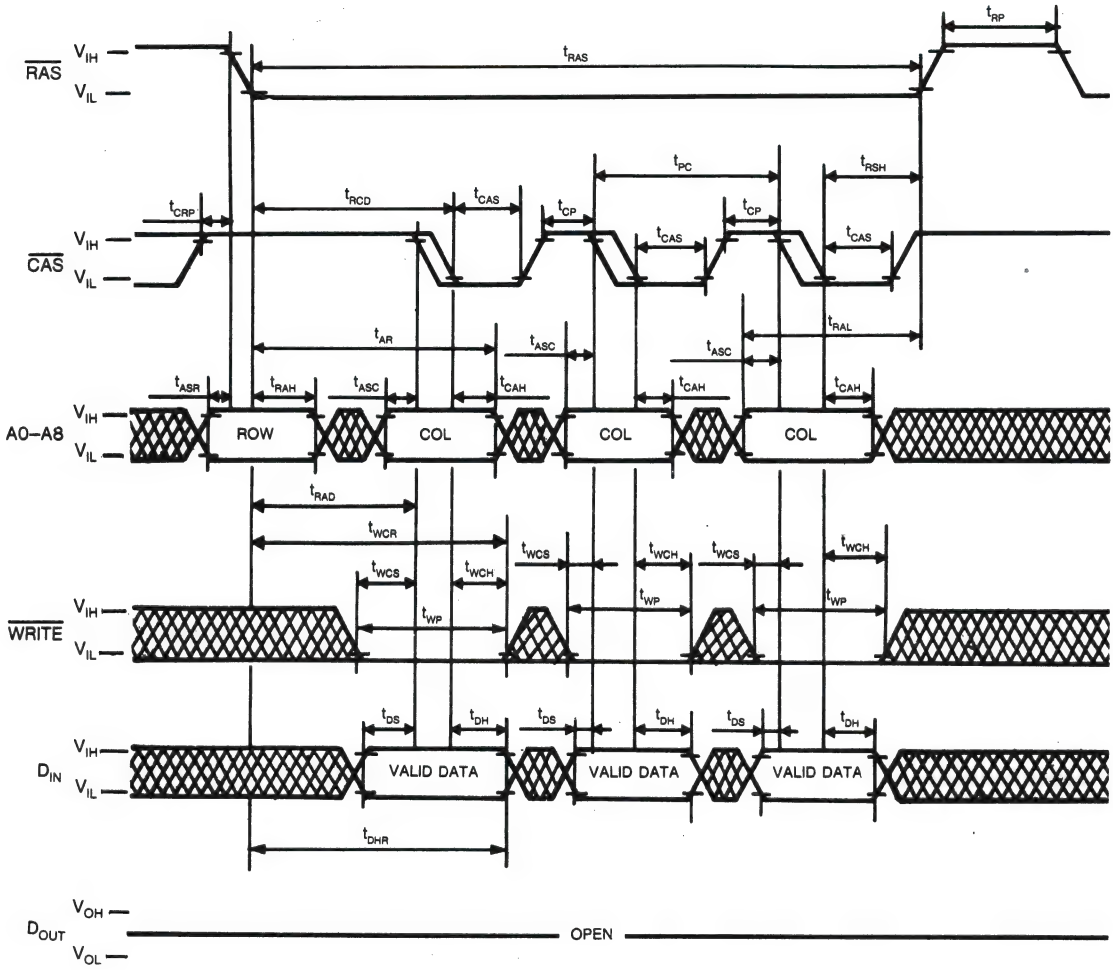


Figure 6. Fast Page Mode Write Cycle (Early Write)

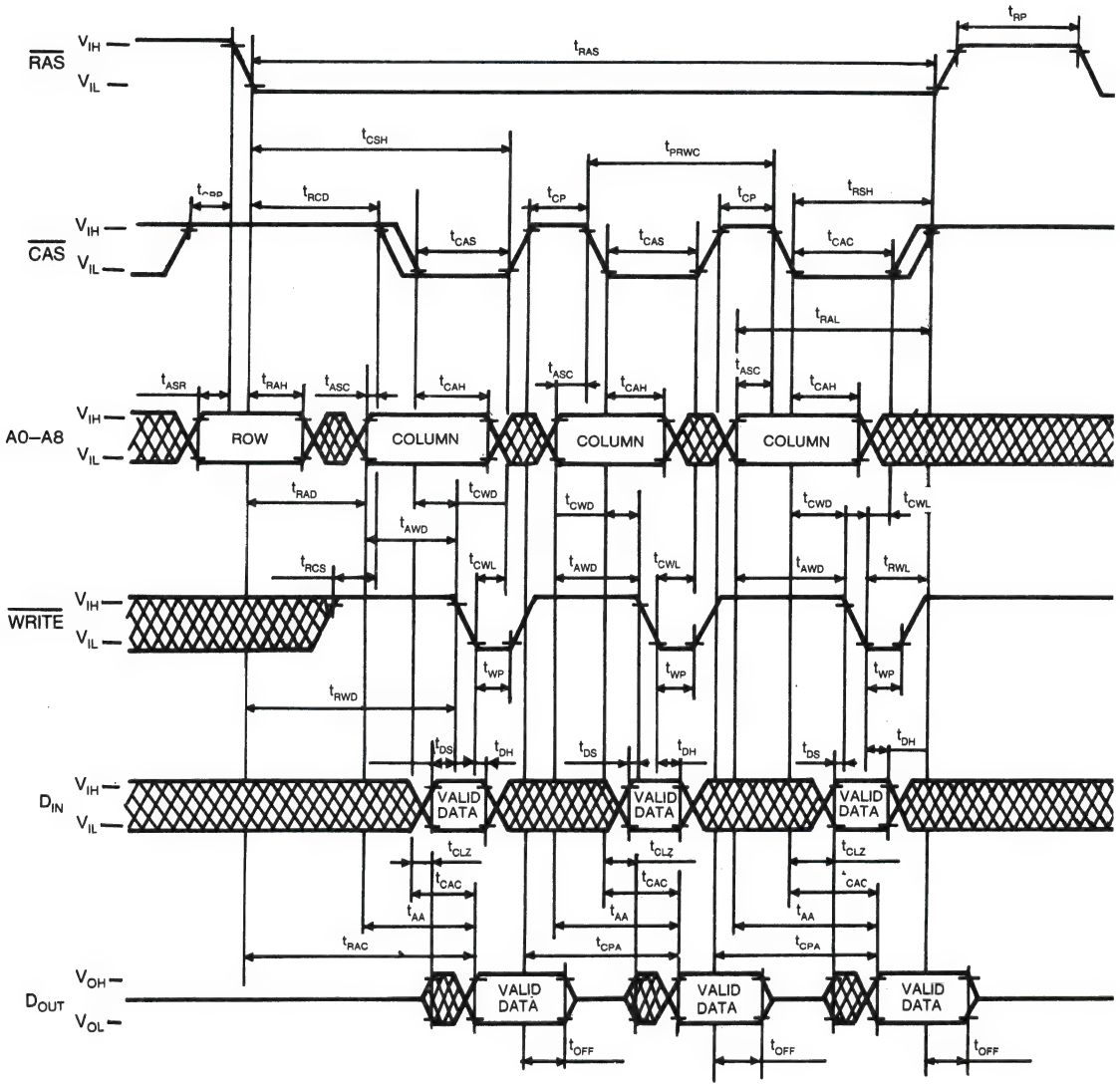


Figure 7. Fast Page Mode Read-Write Cycle

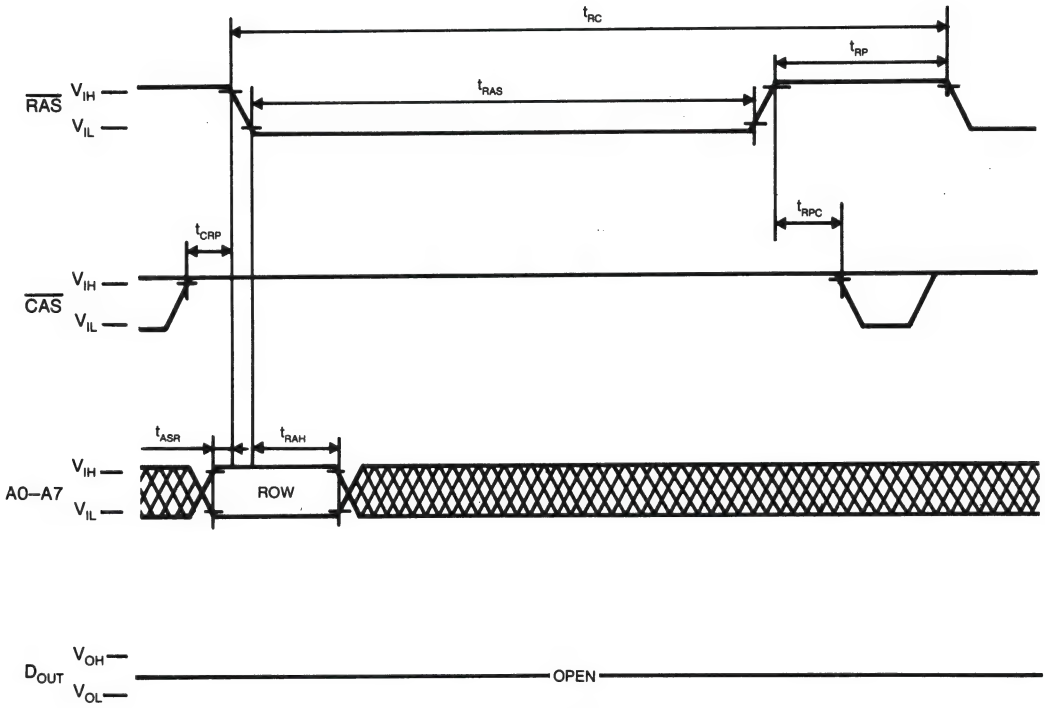


Figure 8. $\overline{RAS}$ Only Refresh Cycle

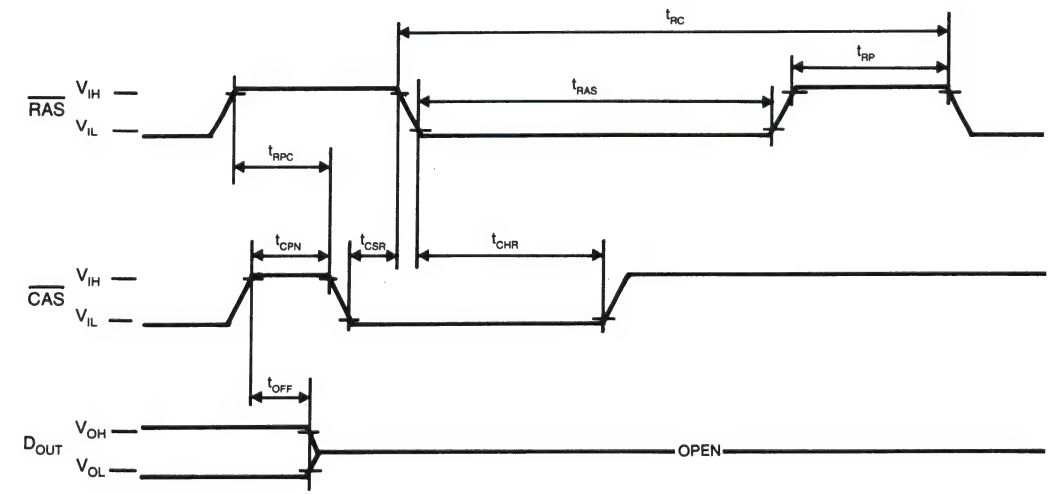


Figure 9. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

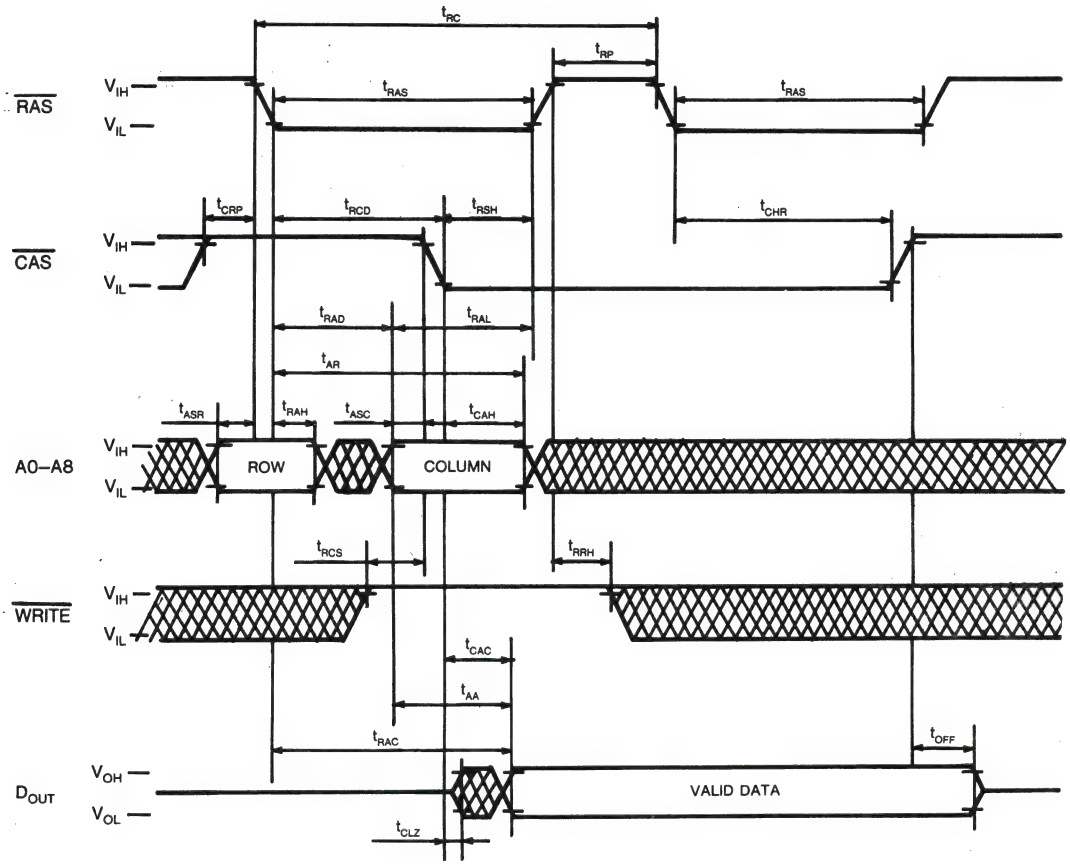


Figure 10. Hidden Refresh Cycle (Read)

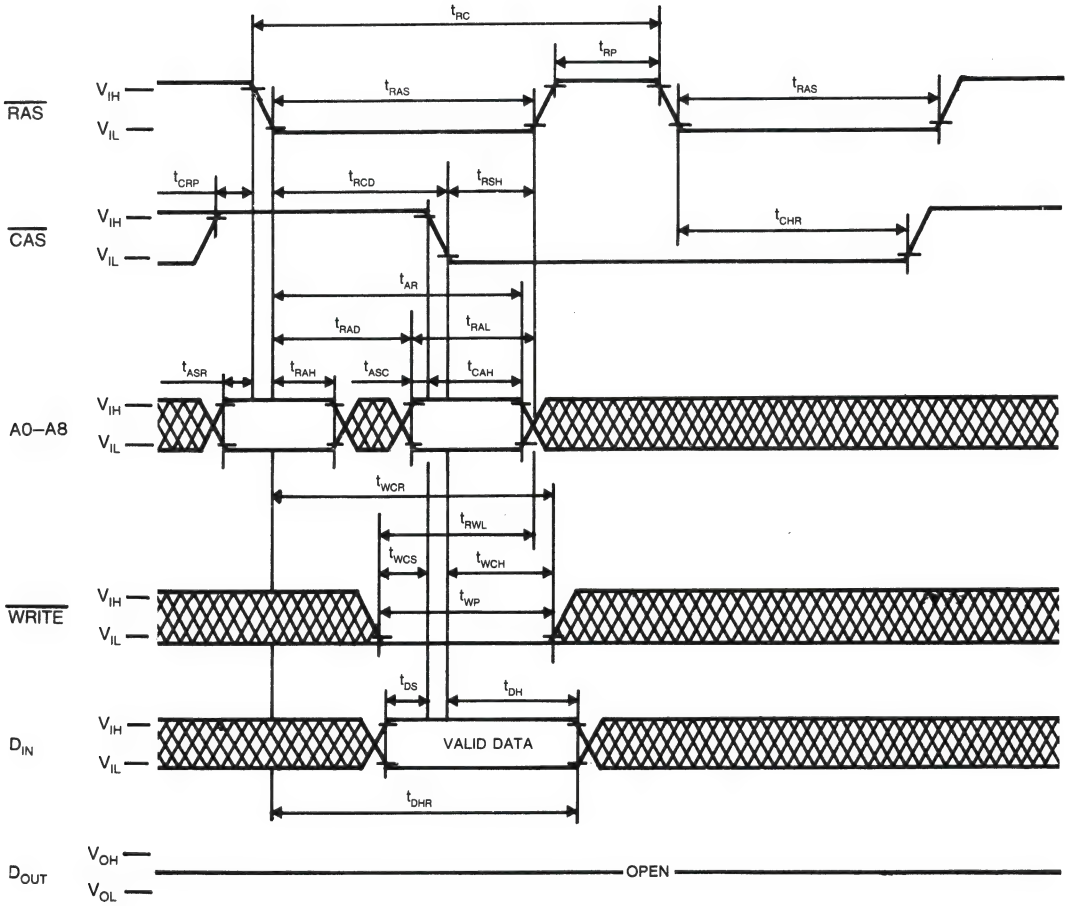


Figure 11. Hidden Refresh Cycle (Write)

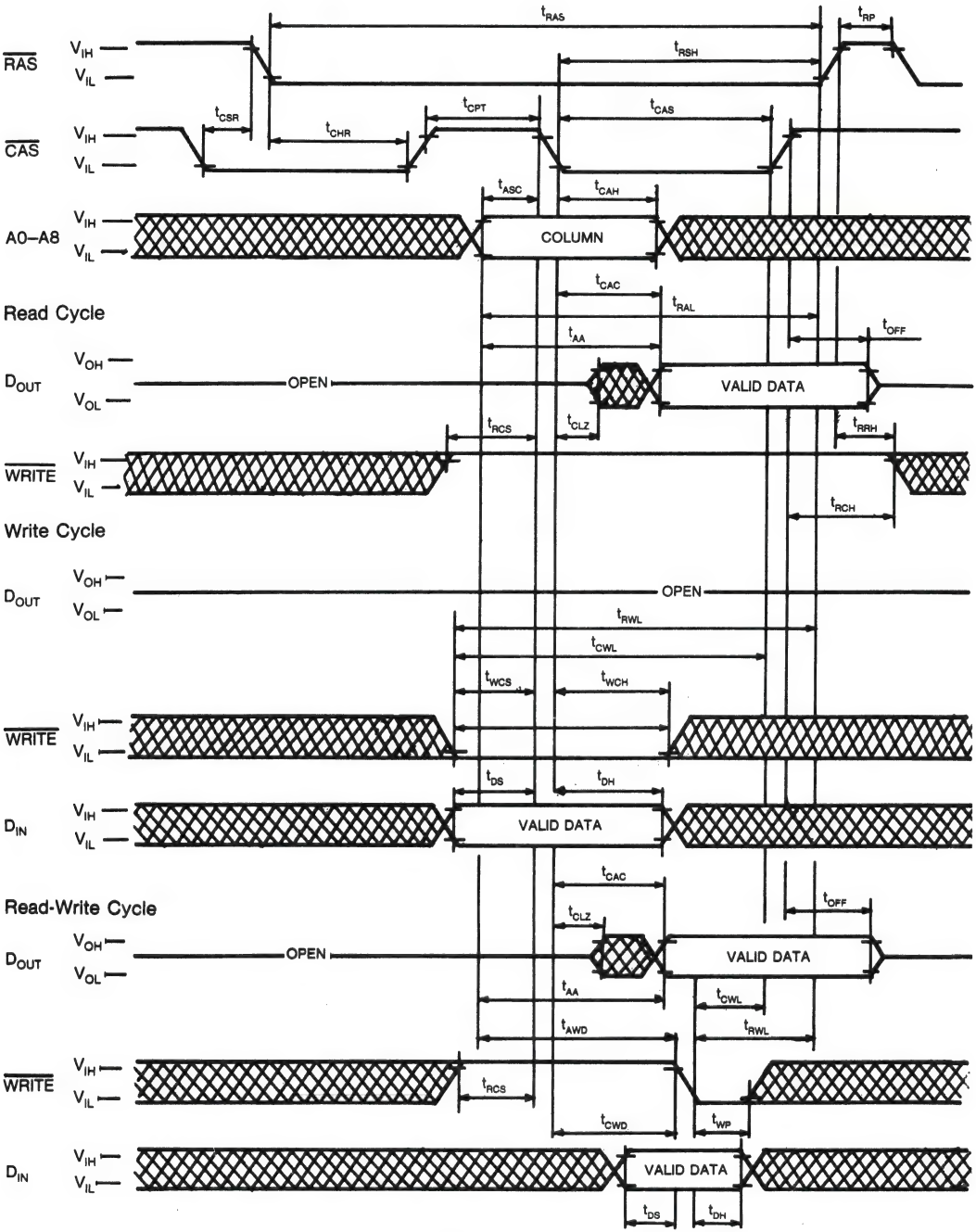


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

GM71C464

65,536WORDS x 4 BIT CMOS DYNAMIC RAM

Description

The GM71C464 is a high speed dynamic RAM organized 65,536 x 4 Bit. The GM71C464 utilizes Goldstar's silicon Gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user The GM71C464 offers Fast Page Mode which allows high speed random access memory cells within the same row. Multiplexed address inputs permit the GM71C464 to be packaged in a standard 18 pin DIP The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The GM71C464 is ideal for high speed, high performance systems such as computer peripherals, control systems, buffer memory and graphic systems.

Features

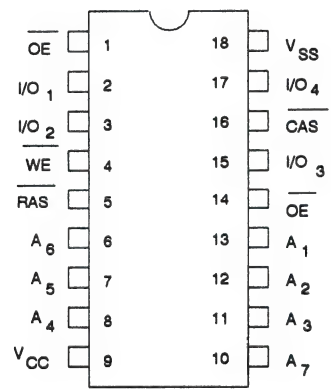
- 65,536 x 4 Bit organization
- Fast access time and cycle time : 80/100/120 ns (Max)
- Single Power Supply of 5V ±10% with a built-in V_{BB} generator
- Performance Range

PARAMETER		GM71C464(ns)		
		-80	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	80	100	120
t_{AA}	Column Address Access Time	40	45	55
t_{CAC}	$\overline{CAS}$ Access Time	30	35	40
t_{RC}	Cycle Time	145	175	205
t_{PC}	Fast Page Mode Cycle Time	55	65	75

- Low Power
  330mW MAX. Operating (GM71C464-80)
  247mW MAX. Operating (GM71C464-12)
  16.5mW MAX. Standby
- Read-Modify-Write, $\overline{RAS}$-only refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh and Fast Page Mode Capability
- All input and output TTL compatible
- 256 refresh cycles/4ms
- Industry standard 18 pin Plastic DIP.

Pin Configuration

18 Plastic DIP



Pin Description

A0 ~ A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply

Ordering Information

Type NO.	Access Time	PKG
GM71C464-80 GM71C464-10 GM71C464-12	80 ns 100 ns 120 ns	300 MIL 18 PIN PLASTIC DIP

Recommended Operating Conditions

(T_A = 0°C to 70°C)

V_{CC} Supply Voltage	4.5 ~ 5.5V
V_{IH} Input High Voltage	2.4 ~ 6.5V
V_{IL} Input Low Voltage (I/O Pin)	-1.0 ~ 0.8V

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to + 70°C
Storage Temperature (plastic)	-55°C to + 125°C
Votage on any Pin Except V_{CC} Relative to V_{SS}	-1.0V to 7.0V
Voltage on V_{CC} relative to V_{SS}	-1.0V to + 7.0V
Data Output Current	50mA
Power Dissipation	1.0W

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	–	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN)	80 100 120	 - 	70 65 60	mA	3, 4
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		-	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN)	80 100 120	 - 	65 55 50	mA	3
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN)	80 100 120	 - 	40 35 30	mA	3, 4
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		-	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	80 10 12	 	65 55 50	mA	
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	80 10 12	 	4 4 4	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 6.5V, All other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 6.5V)		-10	10	µA	

Capacitance (V_{CC} = 5V ±10%, f = 1MHz, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 - A7, D_{IN})	-	4	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	5	pF
C_O	Output Capacitance (I/O_1 - I/O_4)	-	6	pF

*Note : Capacitance is sampled and not 100% TESTED.

Electrical Characteristics and Recommended AC Operating Conditions

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C464-80		GM71C464-10		GM71C464-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	145	-	175	-	205	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	-	265	-	305	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	75	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90	-	100	-	115	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	-	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8, 13
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	55	-	65	ns	8, 14
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	55	-	65	-	75	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	75000	100	75000	120	75000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time (Read or Write Cycle)	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	-	35	-	40		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	65	30	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	25	65	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	20	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	25	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	45	-	55	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	5	-	5	-	5	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5	-	5	-	5	-	ns	10
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	0	-	0	-	0	-	ns	
t_{CLZ}	$\overline{CAS}$ to Low-Z Output	0	-	0	-	0	-	ns	
t_{AR}	Column Address Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{WCR}	Write Command Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{RRW}	$\overline{RAS}$ Pulse Width (RMW)	145	-	175	-	205	-	ns	

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) Unit : nS (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C464-80		GM71C464-10		GM71C464-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	15	-	20	-	25	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	20	-	25	-	ns	11
t_{REF}	Refresh Period (256 cycle)	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to Write Delay Time	55	-	60	-	70	-	ns	12
t_{RWD}	$\overline{RAS}$ to Write Delay Time	110	-	135	-	160	-	ns	12
t_{AWD}	Column Address to Write Delay	70	-	80	-	95	-	ns	12
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	-	30	ns	
t_{OEZ}	Output buffer trun off Delay Time from $\overline{OE}$	0	20	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	25		30	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ Before $\overline{RAS}$ Refresh	25	-	30		40	-	ns	
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	25	-	30	-	35	-	ns	
t_{CORW}	$\overline{CAS}$ Pulse Width (RMW)	95	-	110	-	125	-	ns	
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{CSR}	$\overline{CAS}$ Set up Time $\overline{CBR}$ Refresh	25	-	30	-	40	-	ns	

Notes

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are refrenced to V_{SS}
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μS is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5nS.
7. V_{IH} (min) and V_{IL} (max) are referenced levels for measuring timing of input signals. Also transition times are required between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves the open circuit condition and is not refrenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle: If $t_{RWD} \geq t_{RWD(min)}$, $t_{CWD} \geq t_{CWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$ the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a referenced point only: If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled by t_{CAC}.
14. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a referenced point only: If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

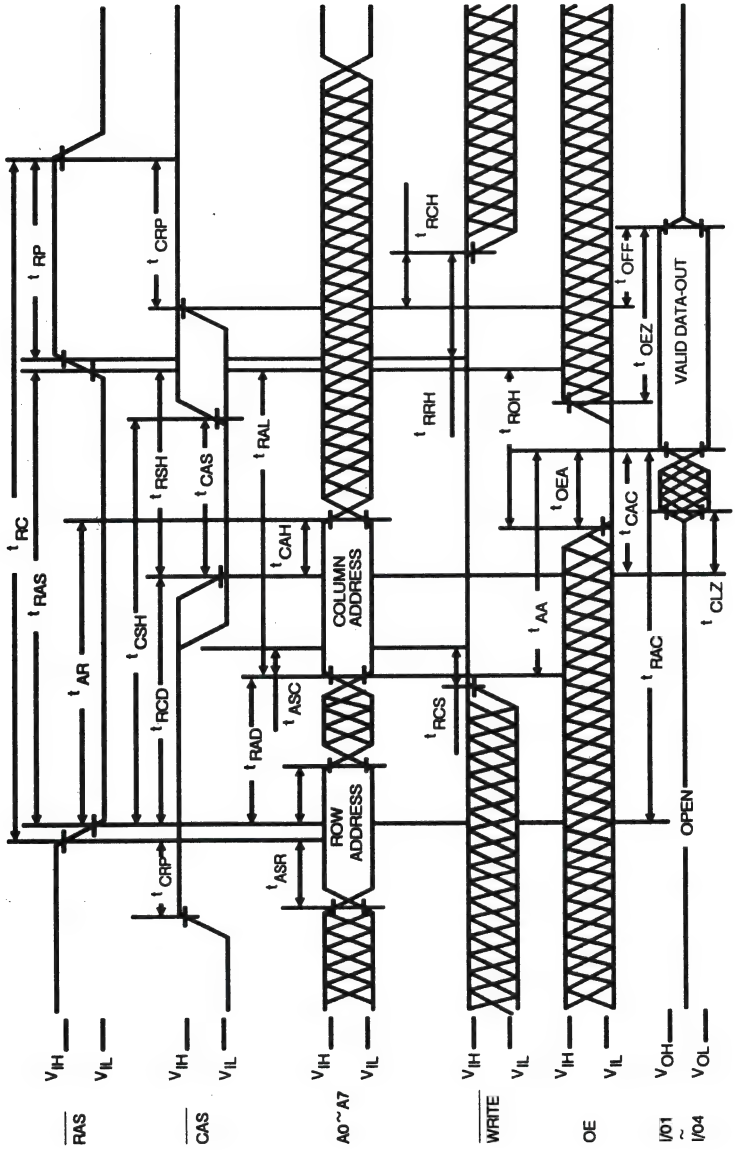


FIGURE 2. READ CYCLE

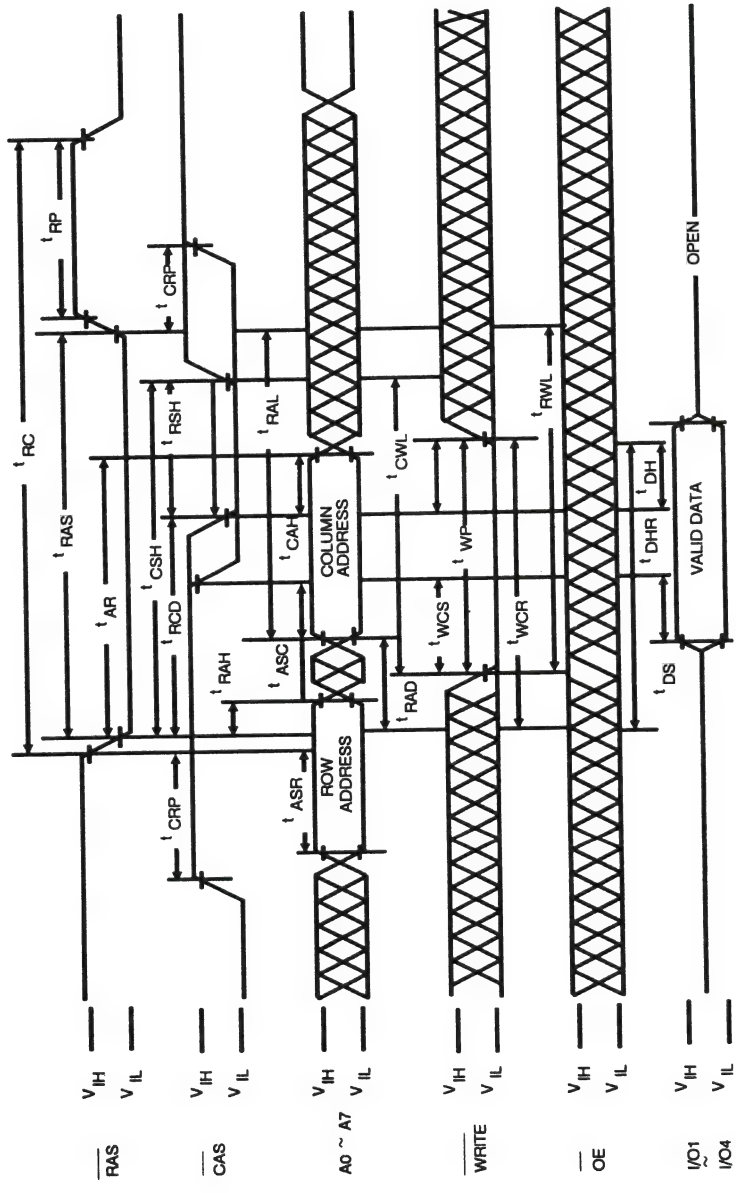


FIGURE 3. WRITE CYCLE (EARLY WRITE)

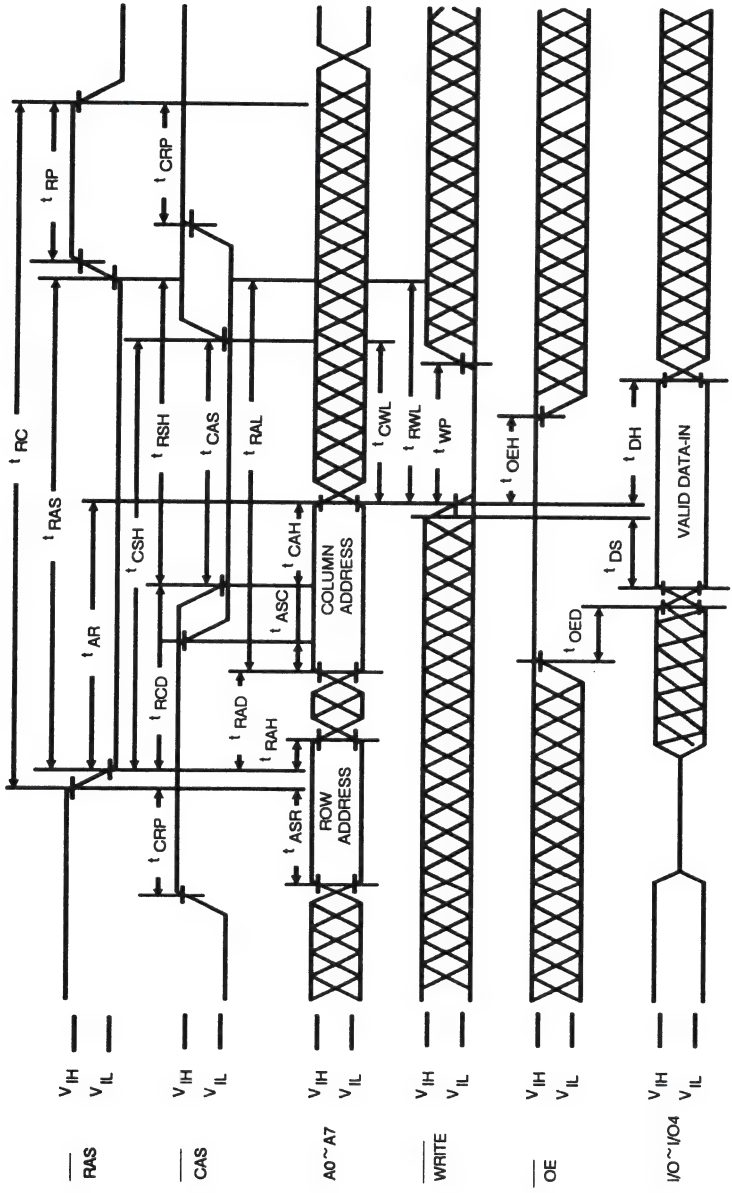


FIGURE 4. WRITE CYCLE (ŌE CONTROLLED WRITE)

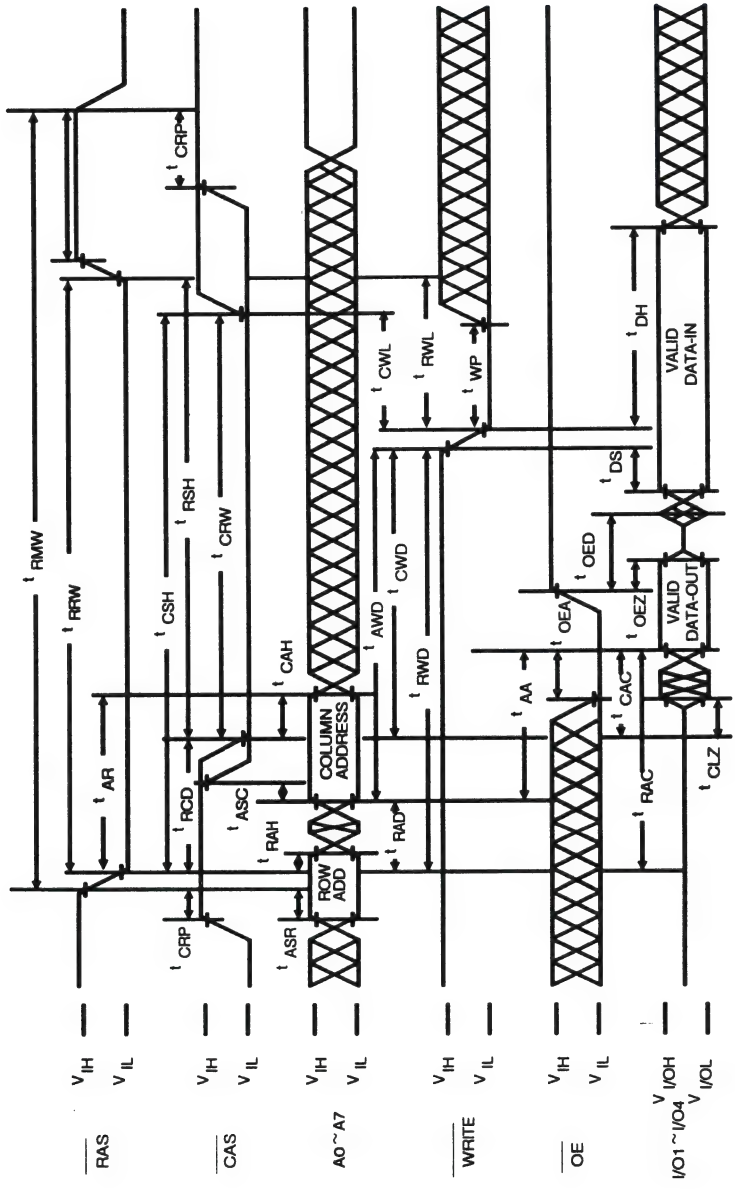


FIGURE 5. READ-MODIFY-WRITE CYCLE

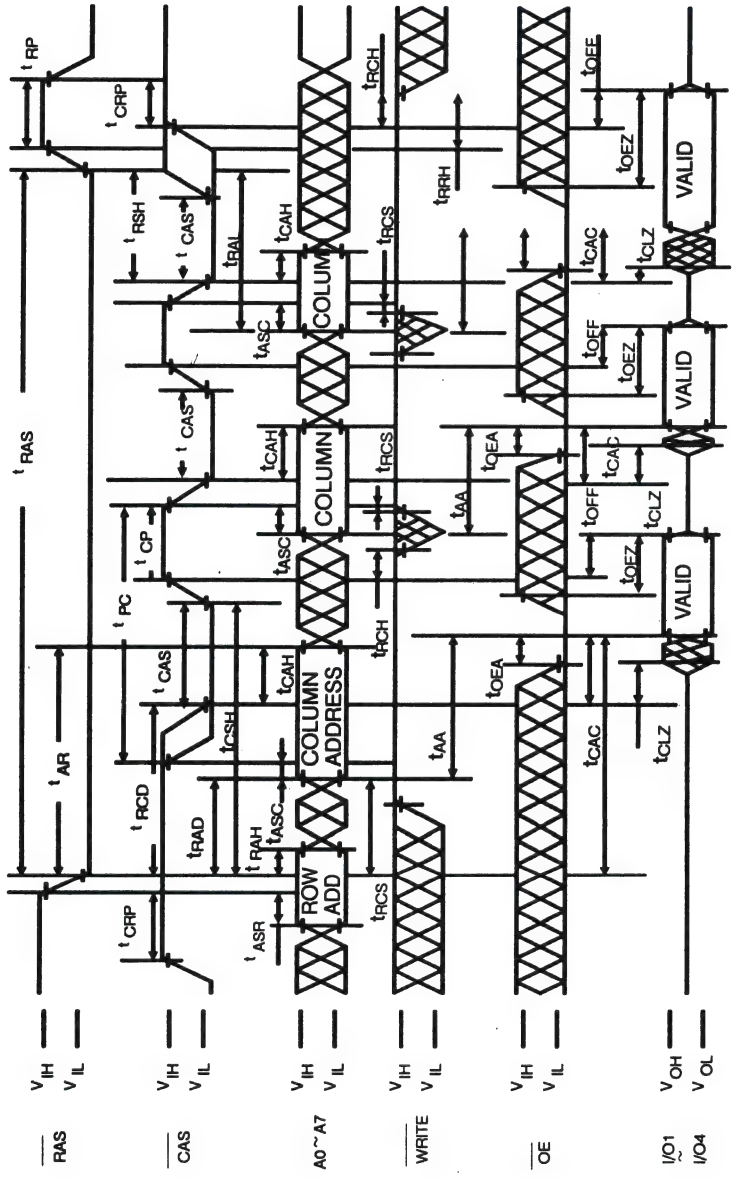


FIGURE 6. FAST PAGE MODE READ CYCLE

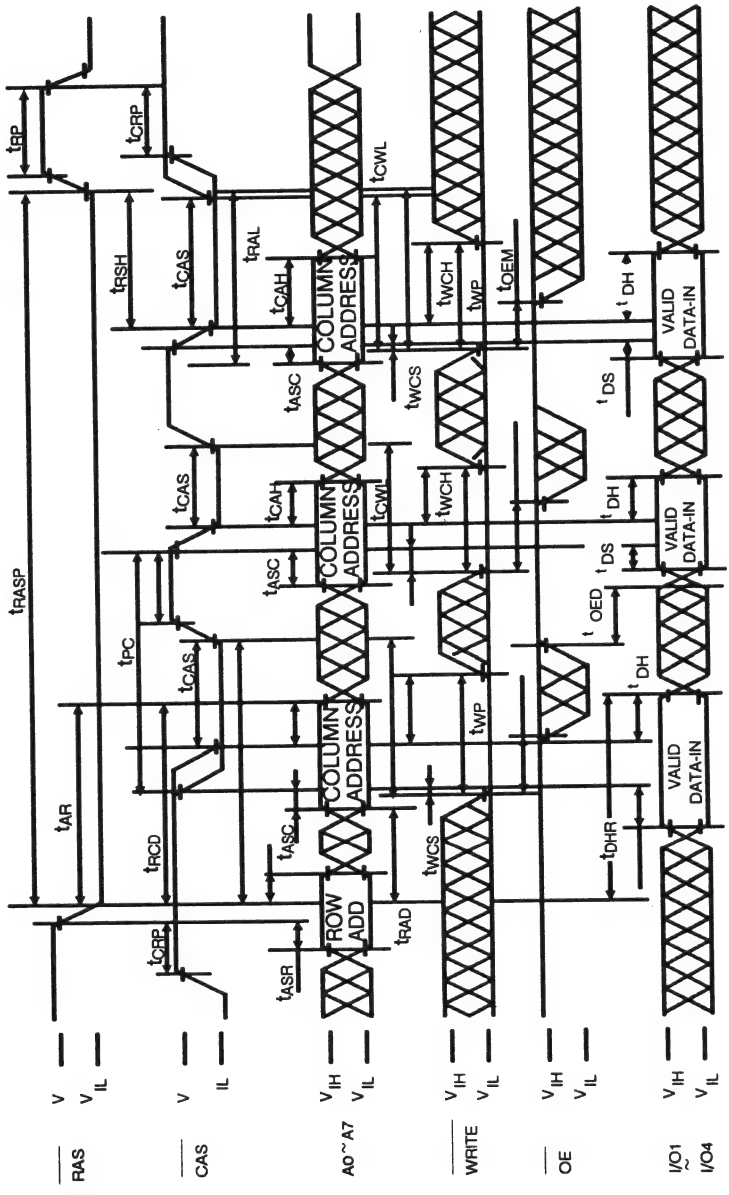


FIGURE 7. FAST PAGE MODE WRITE CYCLE

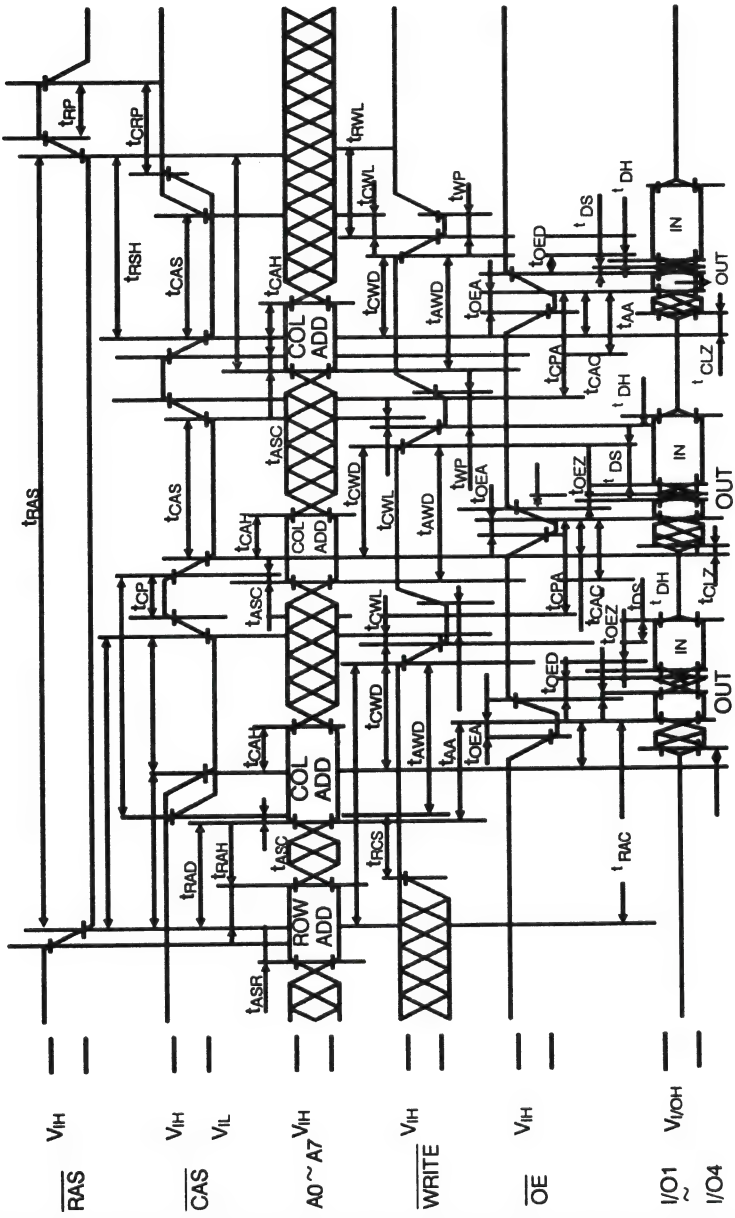


FIGURE 8. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

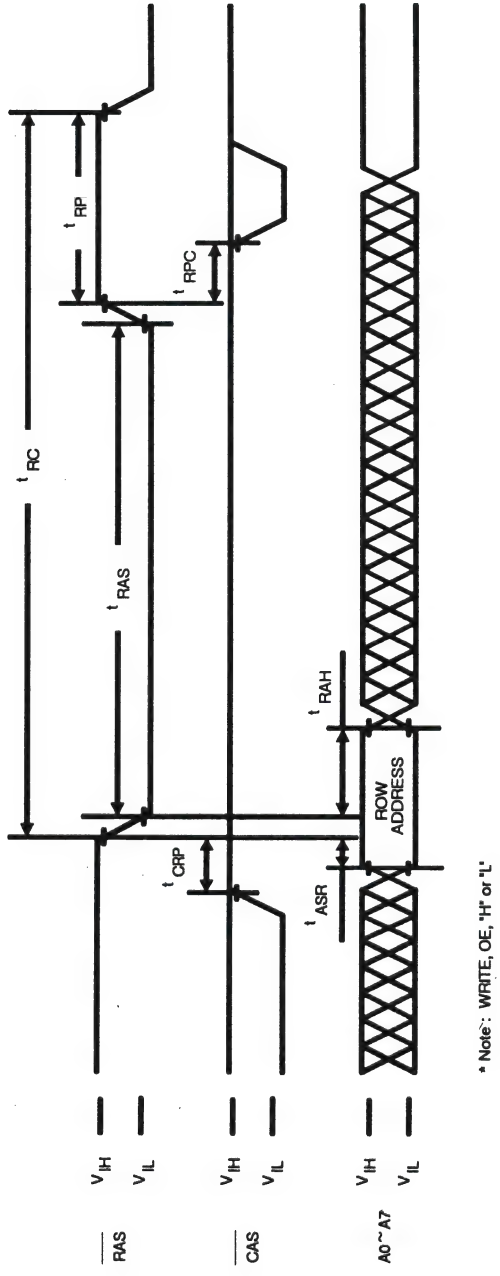
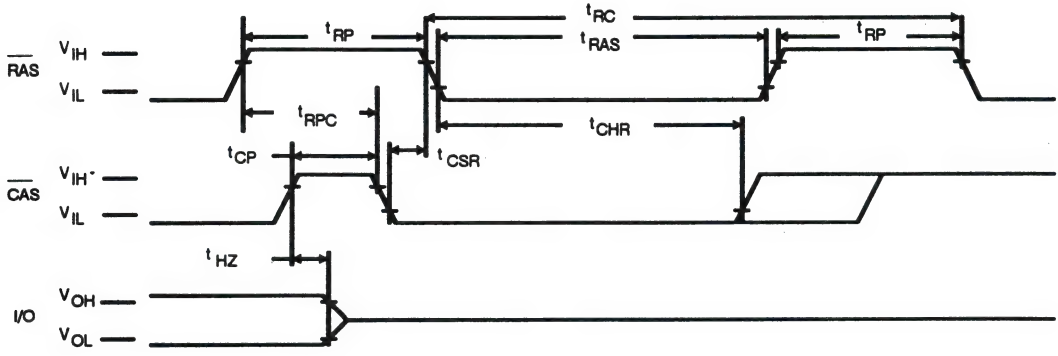


FIGURE 9. $\overline{RAS}$ ONLY REFRESH CYCLE

FIGURE 10. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A0 ~ A7 = Don't care.

FIGURE 11. HIDDEN REFRESH CYCLE (READ)

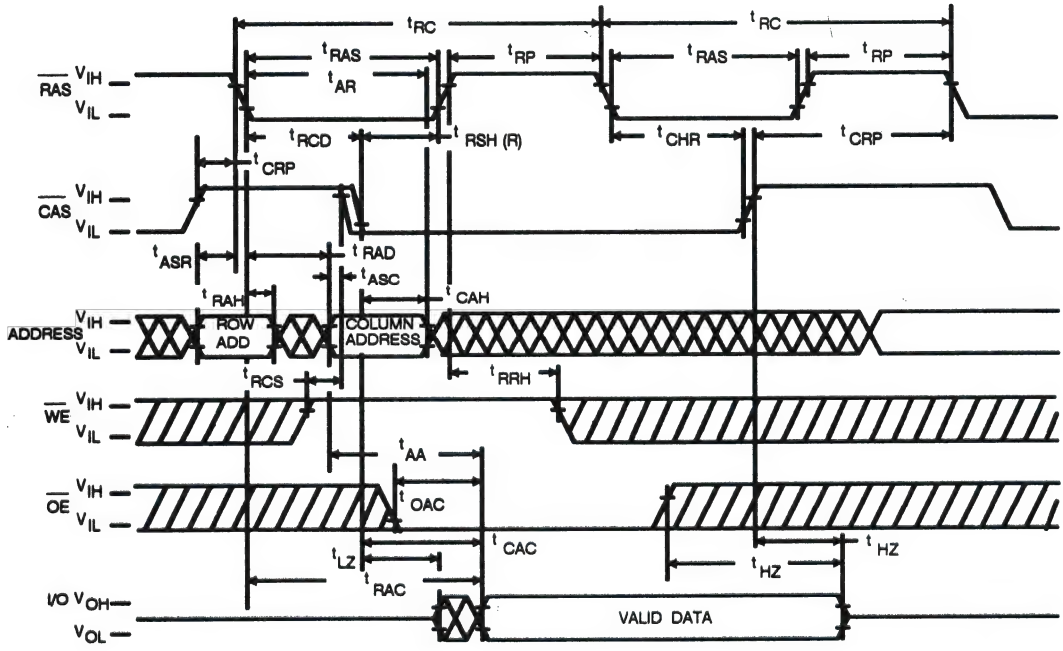


FIGURE 12. HIDDEN REFRESH CYCLE (WRITE)

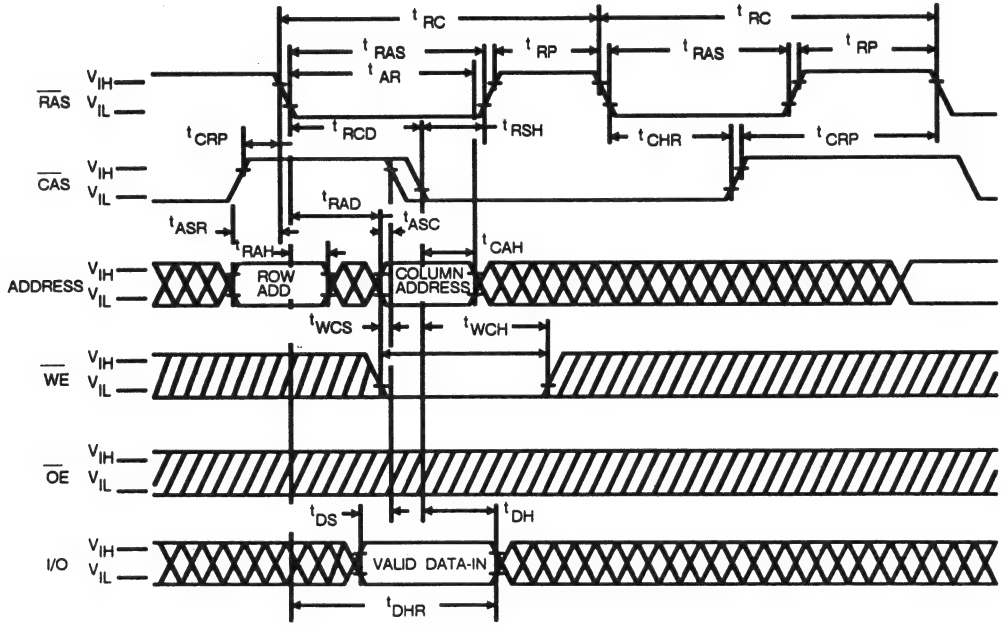
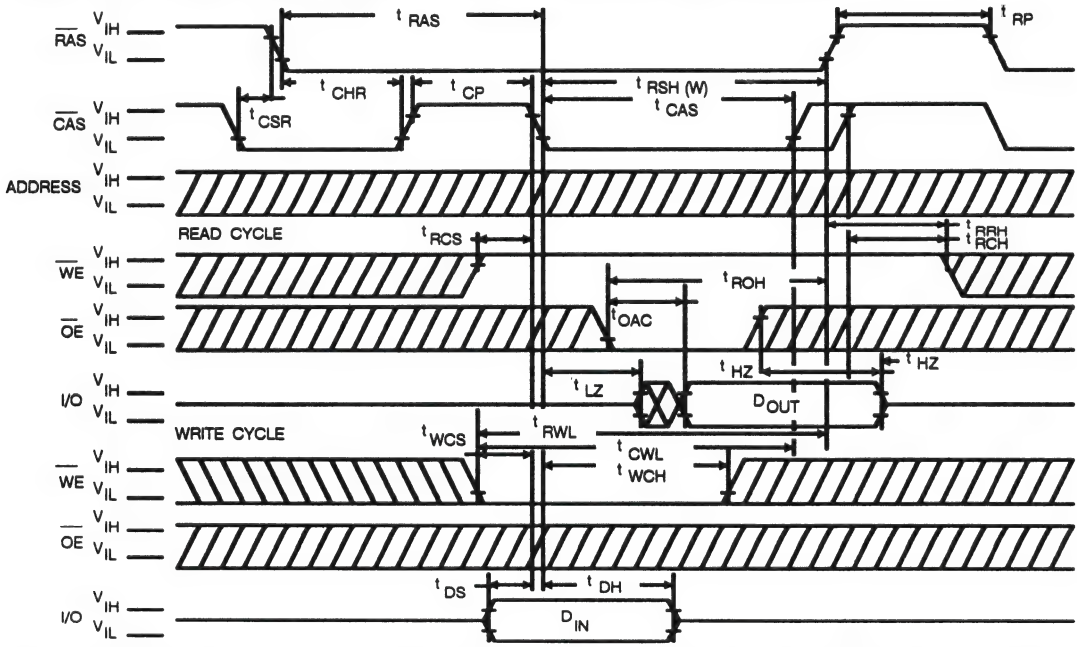


FIGURE 13. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



OBJECTIVE SPECIFICATION

GM71C1000

1,048,576 WORD × 1 BIT HIGH SPEED DYNAMIC RAM

Description

The 71C1000 is the new generation dynamic RAM organized 1,048,576 words by 1bit. The GM71C1000 utilizes Goldstar's silicon gate process technology as well as advanced circuit techniques to provide wide operating margins both internally and to the system user. Multiplexed address inputs permit the GM71C1000 to be packaged in a standard 18 pin DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance direct interfacing capability with high performance logic families such as Schottky TTL.

Feature

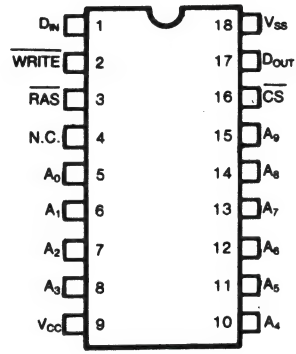
- **1,048,576 words by 1 bit organization**
- **Fast access time and cycle time, 80/100/120ns (Max)**
- **Single power supply of 5V±10% with a built-in V_{BB} generator**
- **Low Power**
  - **385 mW MAX. Operating (GM71C1000-80)**
  - **330 mW MAX. Operating (GM71C1000-10)**
  - **11 mW MAX. Standby**
- **Output unlatched at cycle end allows two-dimensional chip selection**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, Fast Page Mode capability CAS Before RAS Refresh, Hidden Refresh**
- **All inputs and output TTL compatible**
- **512 refresh cycles/8ms**
- **Industry standard 18 pin Plastic DIP/ 20 SOJ/ZIP**

Pin Name

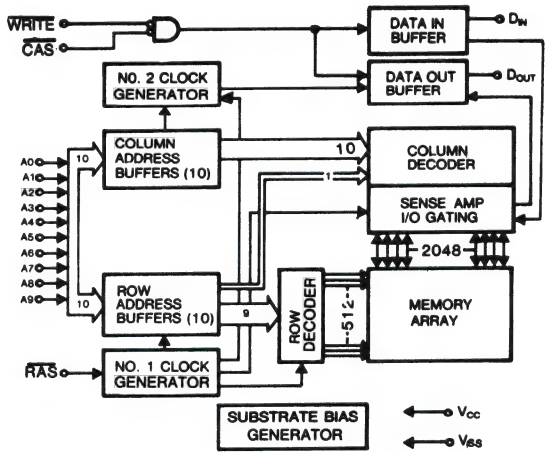
$A_0 \sim A_9$	:	Address Inputs
$\overline{RAS}$	:	Row Address Strobe
D_{IN}	:	Data Input
D_{OUT}	:	Data Output
$\overline{CAS}$	:	Column Address Strobe
$\overline{WRITE}$	:	Read/Write Input
V_{CC}	:	Power (+5V)
V_{SS}	:	Ground
N.C.	:	No Connection

Pin Configuration

(Top View)



Functional Block Diagram



PRELIMINARY SPECIFICATION

GM71C4256
262,144 WORDS × 4 BIT CMOS DYNAMIC RAM

Description

The GM71C4256 is the new generation dynamic RAM organized 262,144 x 4 Bit. The GM71C4256 utilizes GoldStar's silicon Gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the GM71C4256 to be packaged in a standard 20 pin DIP, SOJ and ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

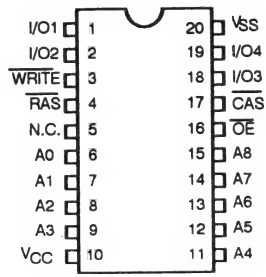
- 262,144 x 4 Bit organization
- Fast access time and cycle time : 85/100/120 (Max)
- Single Power Supply of 5V ± 10% with a built-in V_{BB} generator

PARAMETER		GM71C4256(ns)		
		-85	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	85	100	120
t_{AA}	Column Address Access Time	40	45	55
t_{CAC}	$\overline{CAS}$ Access Time	30	35	40
t_{RC}	Cycle Time	160	190	220
t_{PC}	Fast Page Mode Cycle Time	55	65	75

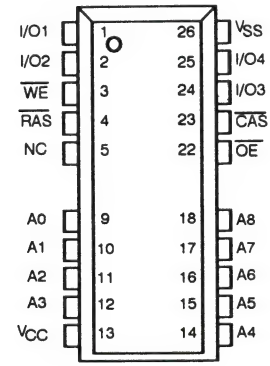
- Low Power
  95mA MAX. Operating (GM71C4256-85)
  70mA MAX. Operating (GM71C4256-12)
  3mA MAX. Standby
- Read-Modify-Write, $\overline{RAS}$-only refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh and Fast Page Mode Capability
- All input and output TTL compatible
- 512 refresh cycles/8ms
- Industry standard 20 pin Plastic DIP/20(26) SOJ/20 ZIP

Pin Configuration

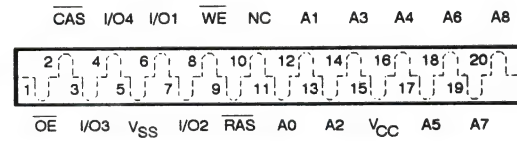
20 Lead Plastic DIP.



20 (26) Lead SOJ Package



20 Lead Plastic ZIP



Pin Description

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Recommended Operating Conditions

(T_A = 0°C to 70°C)

V_{CC} Supply Voltage	4.5 ~ 5.5V
V_{IH} Input High Voltage	2.4 ~ 6.5V
V_{IL} Input Low Voltage	-1.0 ~ 0.8V

Ordering Information

Type NO.	Access Time	PKG
GM71C4256-85 GM71C4256-10 GM71C4256-12	85 ns 100 ns 120 ns	300 MIL 20 PIN PLASTIC DIP
GM71C4256SJ-85 GM71C4256SJ-10 GM71C4256SJ-12	85 ns 100 ns 120 ns	300 MIL 26 (20) PIN PLASTIC SOJ
GM71C4256Z-85 GM71C4256Z-10 GM71C4256Z-12	85 ns 100 ns 120 ns	400 MIL 20 PIN PLASTIC ZIP

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature (plastic)	-55°C to +125°C
Votage on any Pin Except V_{DD} Relative to V_{SS}	-1.0V to +7.0V
Voltage on V_{DD} relative to V_{SS}	-1.0V to +7.0V
Data Output Current	50mA
Power Dissipation	1.0W

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	–	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN)	85 100 120	-	95 80 70	mA	3, 4
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		-	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN)	85 100 120	-	95 80 70	mA	3
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN)	85 100 120	-	50 40 35	mA	3, 4
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		-	3	mA	
I_{CC6}	Standby Current, Output Enabled $\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Other Inputs ≥ V_{SS}			4	mA	
$I_{I(L)}$	Input Leadage Current Any Input (0V ≤ V_{IN} ≤ V_{CC}, All other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	Output Leadage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ V_{CC})		-10	10	µA	

Capacitance* (V_{CC} = 5V ±10%, f = 1MHz, T_A = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 - A8)	-	4	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	5	pF
C_O	Output Capacitance (I/O_1 - I/O_4)	-	6	pF

* Note : Capacitance is sampled and not 100% tested.

Electrical Characteristics And Recommended AC Operating Conditions

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C4256-85		GM71C4256-10		GM71C4256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	160	-	190	-	220	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	-	265	-	305	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	75	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	115	-	135	-	155	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8, 13
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	55	-	65	ns	8, 14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	65	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	85,000	100	85,000	120	85,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	85,000	100	85,000	120	85,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time (Read or Write Cycle)	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	-	35	-	40	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	30	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	45	20	55	25	65	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	-	15	-	15	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time	5	-	5	-	5	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5	-	5	-	5	-	ns	10
t_{RRW}	Read-Modify-Write Cycle Time $\overline{RAS}$ Pulse Width	150	-	175	-	205		ns	

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) Unit : nS (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C4256-85		GM71C4256-10		GM71C4256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	15	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{REF}	Refresh Period (512 cycle)	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to Write Delay Time	60	-	70	-	80	-	ns	12
t_{RWD}	$\overline{RAS}$ to Write Delay Time	115	-	135	-	160	-	ns	12
t_{AWD}	Column Address to Write Delay	70	-	80	-	85	-	ns	12
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	0	-	0	-	0	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	-	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	-	30	-	35	-	ns	
t_{OEZ}	Output buffer trun off Delay Time from $\overline{OE}$	0	20	0	25	0	30 -	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	25	-	30	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ Before $\overline{RAS}$ Refresh	25		30		40		ns	

Notes

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltage are refrenced to V_{SS}
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 µS is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5nS.
7. V_{IH} (min) and V_{IL} (max) are referenced levels for measuring timing of input signals. Also transition times are required between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves the open circuit condition and is not refrenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t WCS, tRWD, tCWD and tA /D are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle: If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min) the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a referenced point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by tCAC.
14. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a referenced point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by tAA.

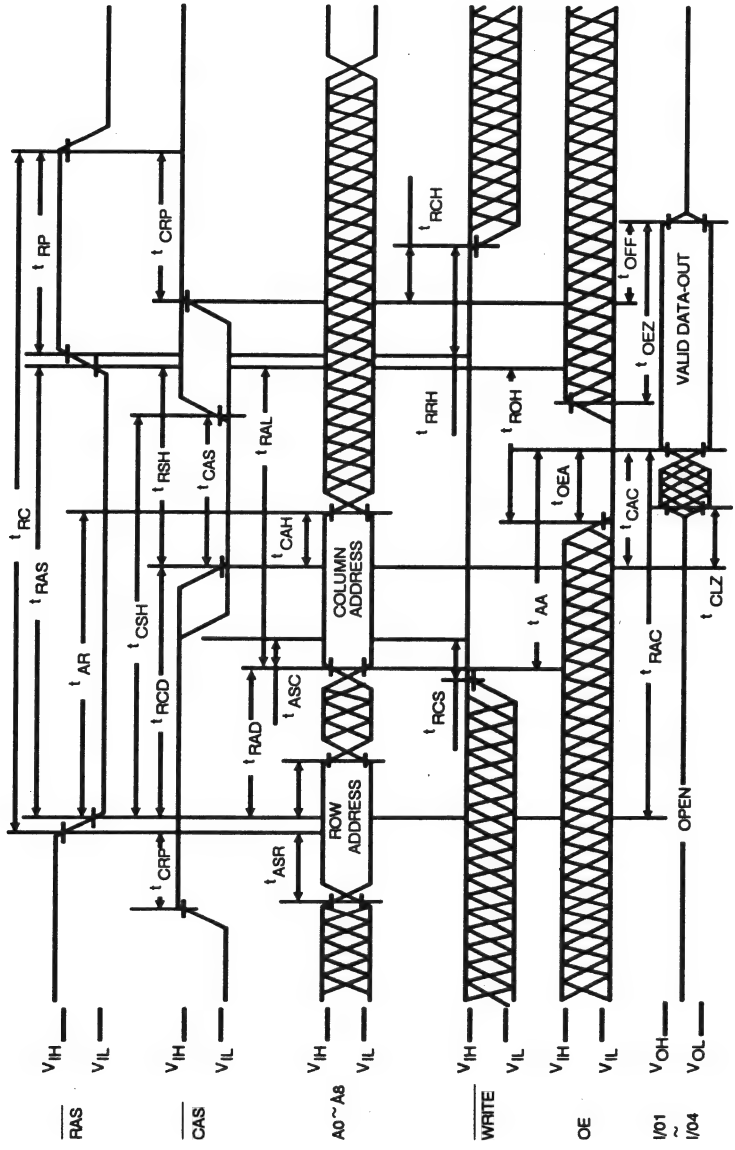


FIGURE 2. READ CYCLE

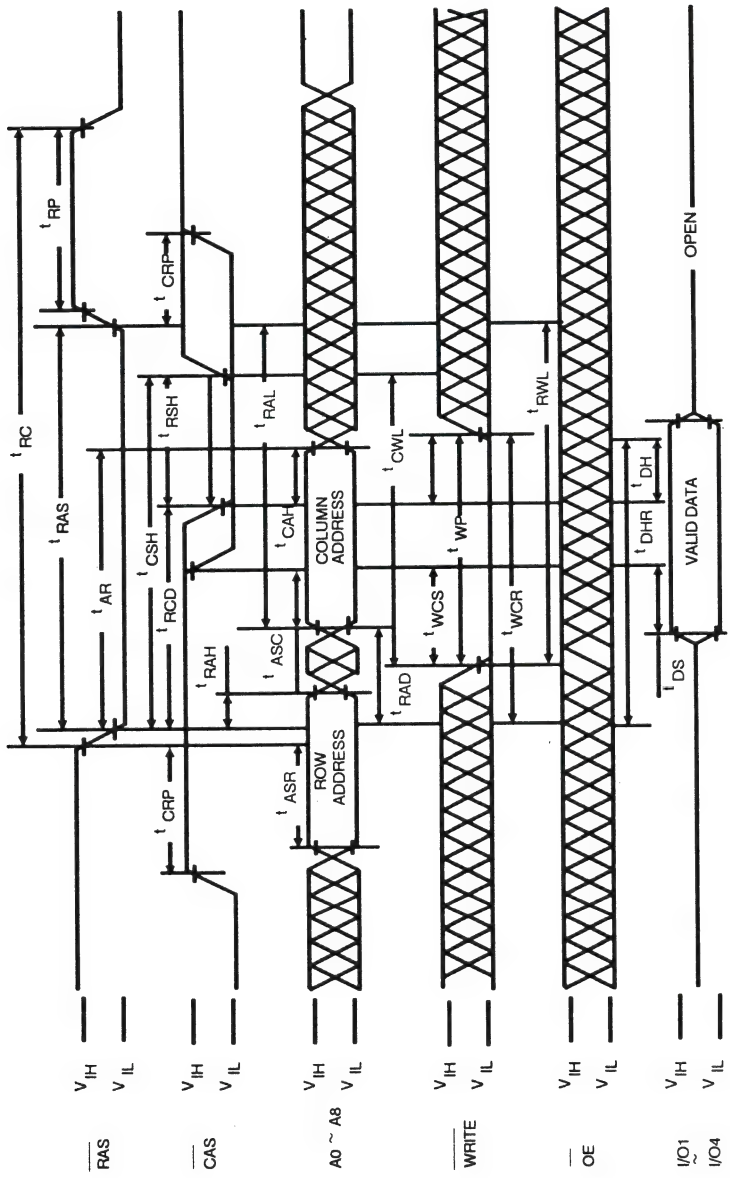


FIGURE 3. WRITE CYCLE (EARLY WRITE)

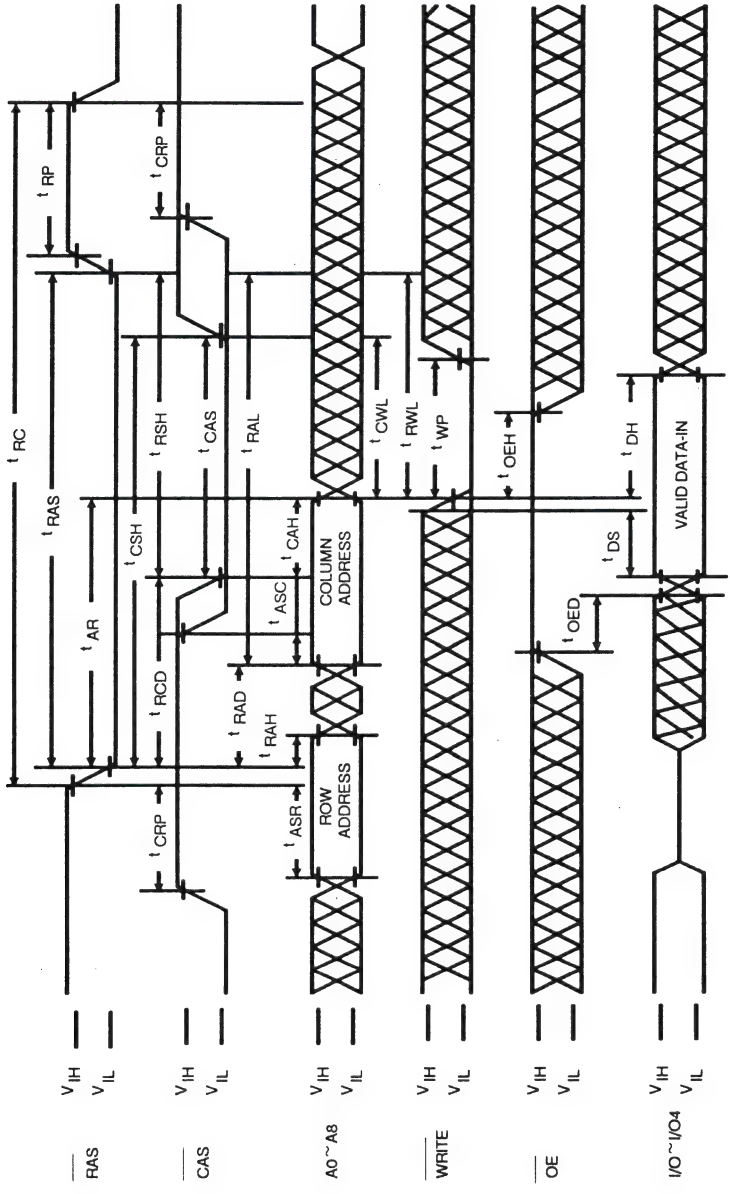


FIGURE 4. WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

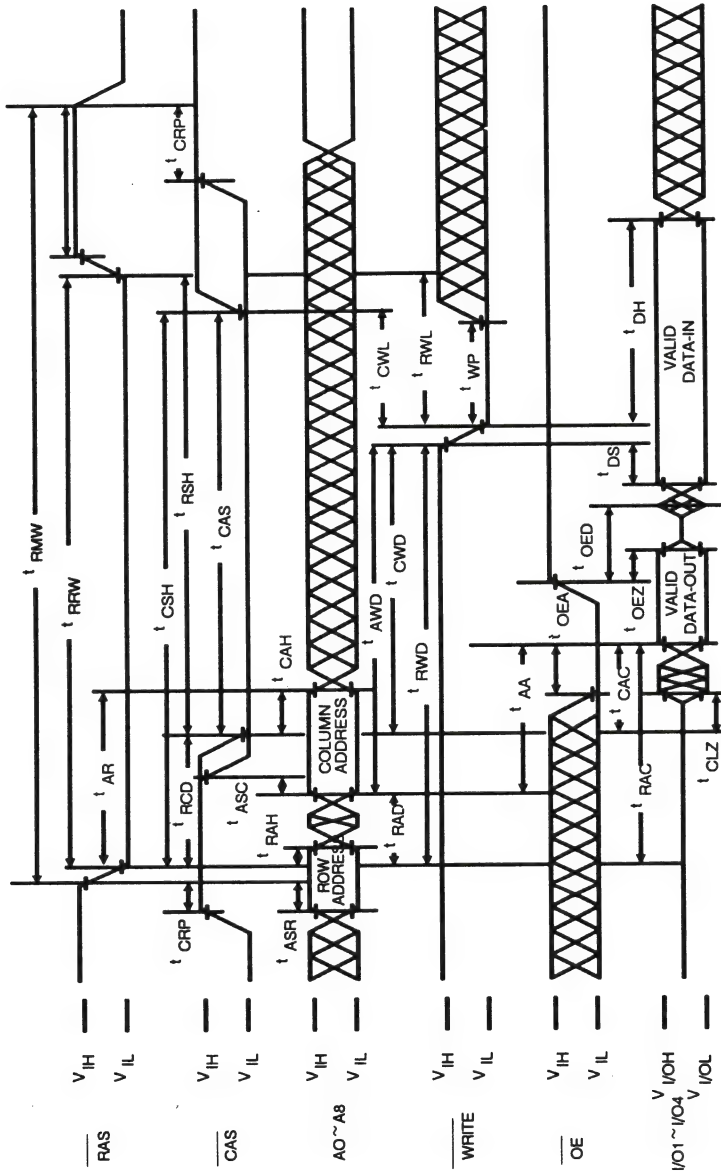


FIGURE 5. READ-MODIFY-WRITE CYCLE

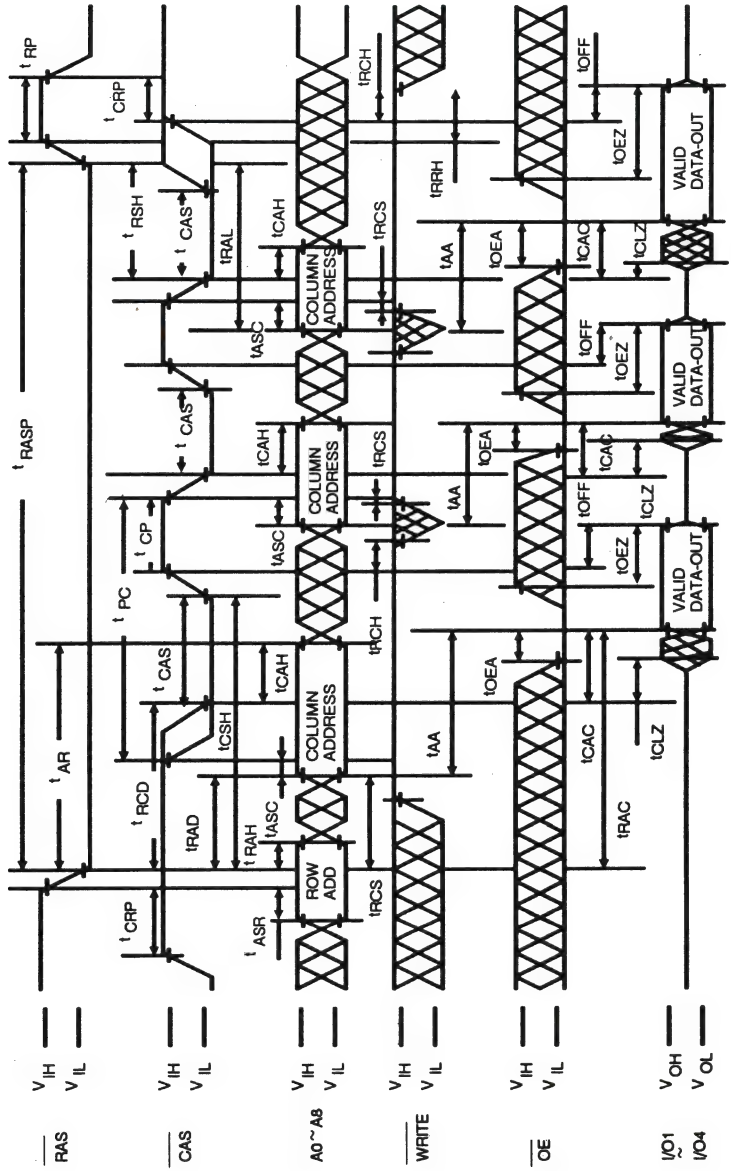


FIGURE 6. FAST PAGE MODE READ CYCLE

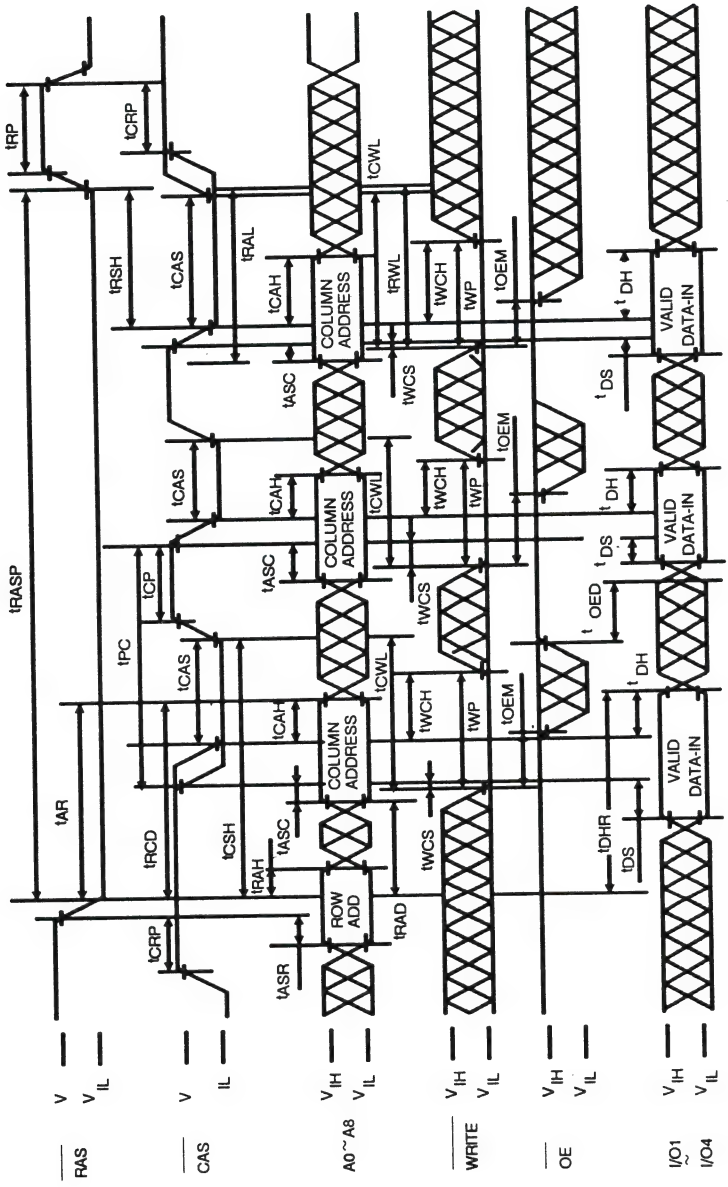


FIGURE 7. FAST PAGE MODE WRITE CYCLE

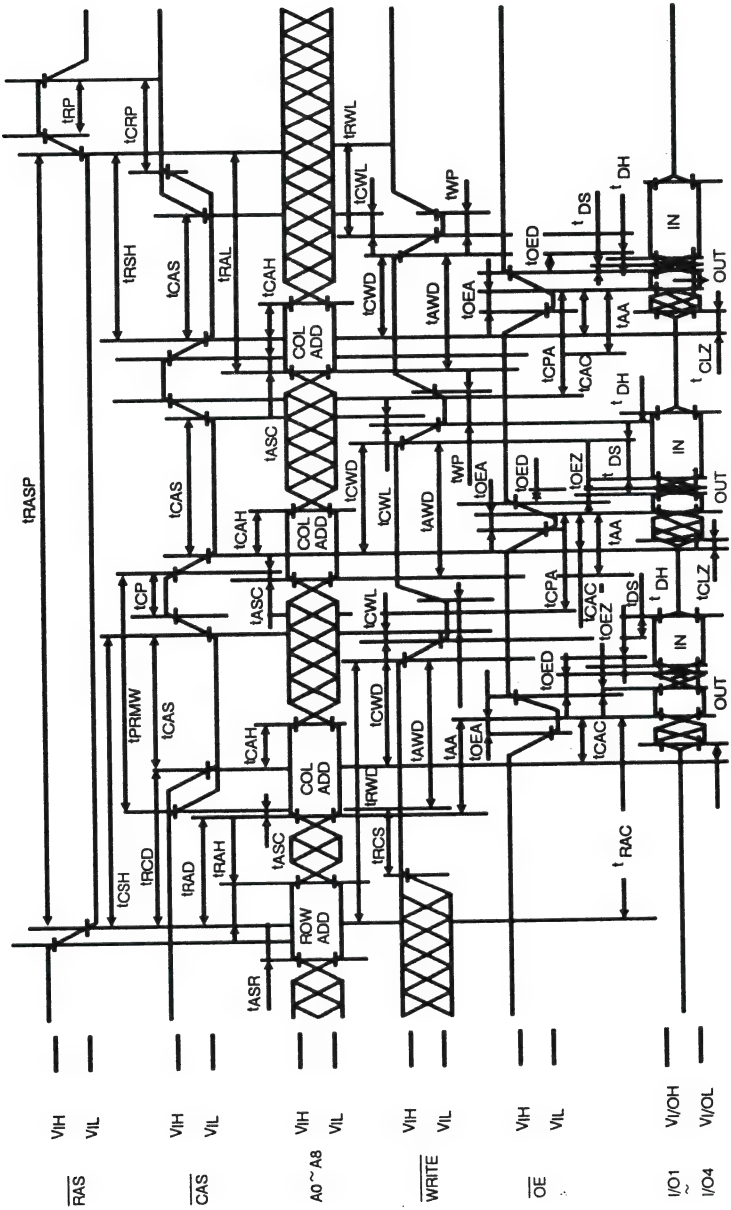


FIGURE 8. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

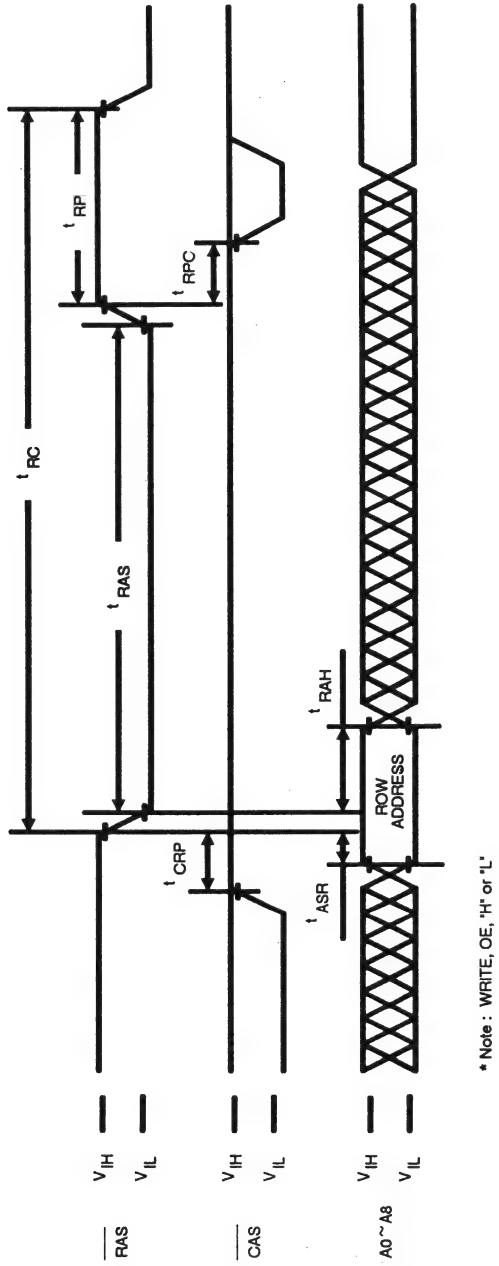
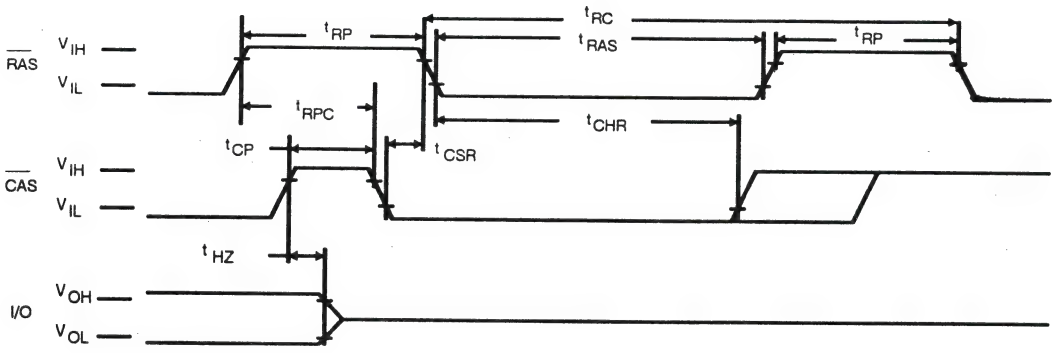


FIGURE 9. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

FIGURE 10. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 ~ A7 = Don't care.

FIGURE 11. HIDDEN REFRESH CYCLE (READ)

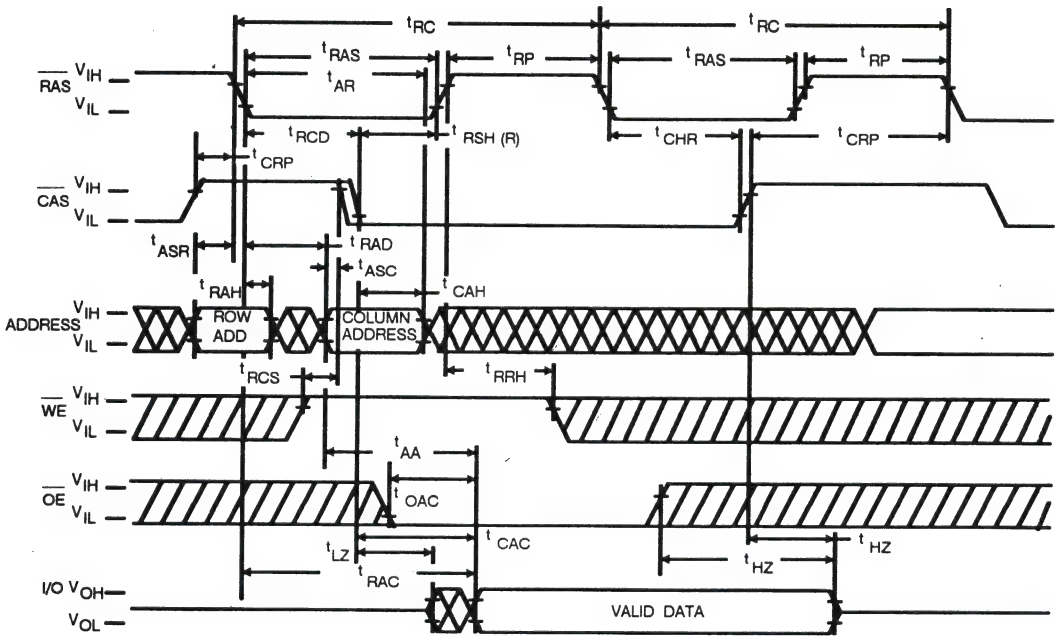


FIGURE 12. HIDDEN REFRESH CYCLE (WRITE)

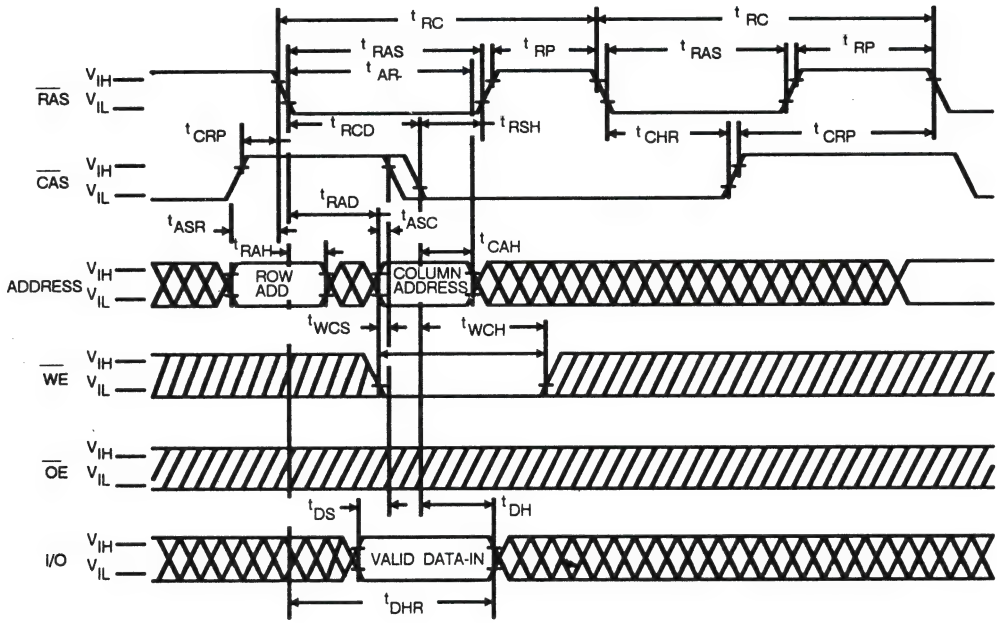
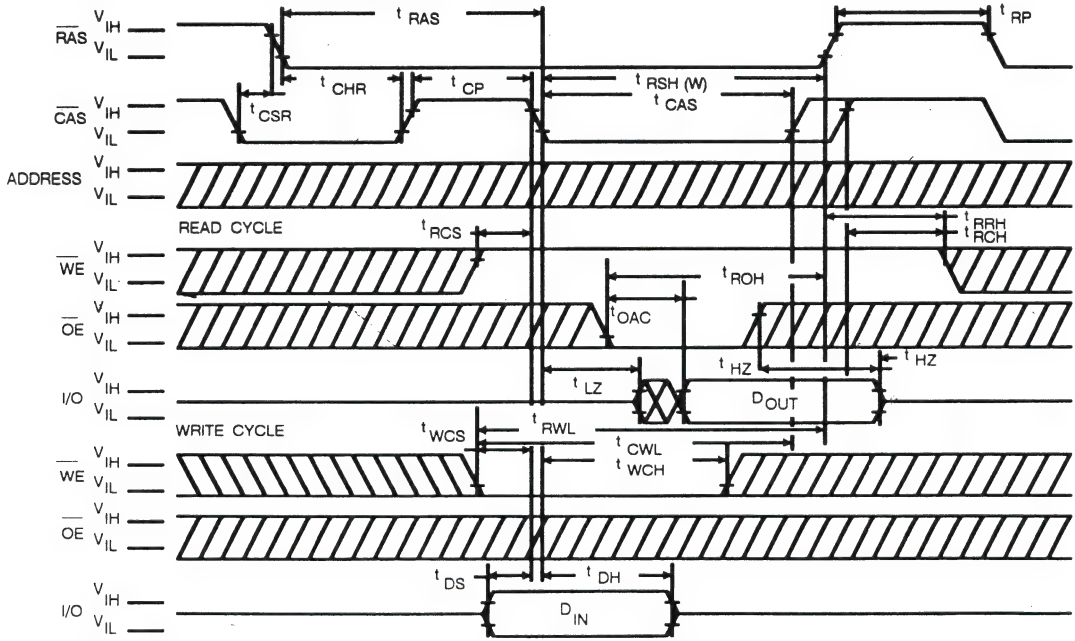


FIGURE 13. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

The GM71C4256 is a CMOS dynamic RAM optimized for high data bandwidth low power applications. It is functionally similar to a traditional dynamic RAM.
The GM71C4256 reads and writes data by multiplexing a 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily depedent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

MEMORY CYCLE

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{AA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{AA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

WRITE CYCLE

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The colunm address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state. In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

REFRESH CYCLE

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 rew addresses (A0 through A8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$ only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The GM71C4256 will use the output of an internal 9-bit counter as the source or row addresses and ignore external address inputs.
$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output will remain in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

DATA RETENTION MODE

The GM71C4256 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{CC}. While the $\overline{RAS}$ clocik is at the "extra high" level, the GM71C4256 power consumption is reduced to the low I_{CC6} level. Overall I_{CC} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{ACTIVE}) + (t_{RX} - t_{RC}) \times (I_{CC6})}{t_{RX}}$$

Where : t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

FAST PAGE MODE OPERATION

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to re-apply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the failing edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{AA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{AA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 18 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

DATA OUTPUT OPERATION

The GM71C4256 Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

POWER ON

After application of the V_{CC} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycle containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During power on, the V_{CC} current requirement of the GM71C4256 is dependant on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power On, the device will go into an active cycle and I_{CC} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power On to avoid current surges.

TABLE 1. DATA OUTPUT

Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

PRELIMINARY SPECIFICATION

GM71C4256A
262,144 WORDS x 4 BIT CMOS DYNAMIC RAM

Description

The GM71C4256A is the new generation dynamic RAM organized 262,144 x 4 Bit. GM71C4256A has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4256A offers Fast Page Mode as a high speed access Mode. Multiplexed address inputs permit the GM71C4256A to be packaged in a standard 20 pin DIP, SOJ and ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

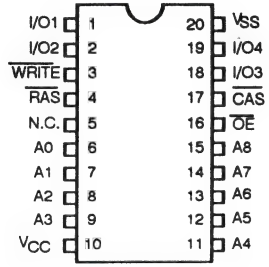
- 262,144 x 4 Bit organization
- Fast access time and cycle time : 80/100/120 (Max)
- Single Power Supply of 5V ± 10% with a built-in V_{BB} generator

PARAMETER		GM71C4256A(ns)		
		-80	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	80	100	120
t_{AA}	Column Address Access Time	40	45	55
t_{CAC}	$\overline{CAS}$ Access Time	25	25	30
t_{RC}	Cycle Time	160	190	220
t_{PC}	Fast Page Mode Cycle Time	55	55	65

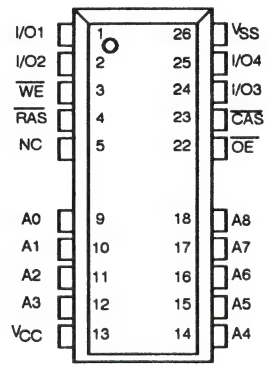
- Low Power
  363mW MAX. Operating (GM71C4256A-80)
  303mW MAX. Operating (GM71C4256A-10)
  259mW MAX Operating (GM71C4256A-12)
  11mW MAX. Standby
- Read-Modify-Write, $\overline{RAS}$-only refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh and Fast Page Mode Capability
- All input and output TTL compatible
- 512 refresh cycles/8ms
- Industry standard 20 pin Plastic DIP/20(26) SOJ/20 ZIP

Pin Configuration

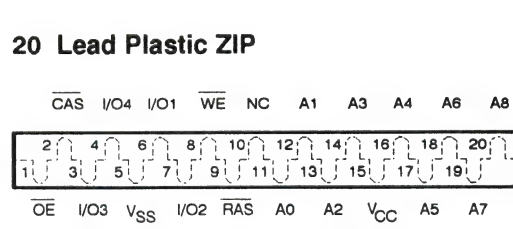
20 PLASTIC DIP



20 (26) Lead SOJ Package



20 Lead Plastic ZIP



Pin Description

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Recommended Operating Conditions

(T_A = 0°C to 70°C)

V_{CC}	Supply Voltage	4.5 ~ 5.5V
V_{IH}	Input High Voltage	2.4 ~ 6.5V
V_{IL}	Input Low Voltage (I/O Pin)	-1.0 ~ 0.8V
	Input Low Voltage (Others)	-2.0 ~ 0.8V

Ordering Information

Type NO.	Access Time	PKG
GM71C4256A-80 GM71C4256A-10 GM71C4256A-12	80 ns 100 ns 120 ns	300 MIL 20 PIN PLASTIC DIP
GM71C4256ASJ-80 GM71C4256ASJ-10 GM71C4256ASJ-12	80 ns 100 ns 120 ns	300 MIL 20 PIN (26) PLASTIC SOJ
GM71C4256AZ-80 GM71C4256AZ-10 GM71C4256AZ-12	80 ns 100 ns 120 ns	400 MIL 20 PIN PLASTIC ZIP

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature (plastic)	-55°C to +125°C
Votage on any Pin Except V_{CC} Relative to V_{SS}	-1.0V to +7.0V
Voltage on V_{CC} relative to V_{SS}	-1.0V to +7.0V
Data Output Current	50mA
Power Dissipation	1.0W

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	–	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN)	80 100 120	- -	66 55 47	mA	3, 4
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN)	80 100 120	- -	66 55 47	mA	3
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN)	80 100 120	- -	55 55 47	mA	3, 4
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	80 10 12		66 55 47	mA	
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	80 10 12		5 5 5	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V, All other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		-10	10	µA	

Capacitance (V_{CC} = 5V ±10%, f = 1MHz, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 - A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Output Capacitance (I/O_1 - I/O_4)	-	10	pF

* Note : Capacitance is sampled and not 100% tested.

Electrical Characteristics And Recommended AC Operating Conditions

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C4256A-80		GM71C4256A-10		GM71C4256A-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	160	-	190	-	220	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	220	-	255	-	295	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	55	-	65	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	110	-	115	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	-	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8, 13
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	50	-	60	ns	8, 14
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000	120	10000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	10000	-	10000	-	10000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time (Read or Write Cycle)	25	-	25	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000	30	10000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	22	55	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	17	40	20	55	20	65	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	12	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	45	-	55	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	10	-	10	-	10	-	ns	10

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) Unit : nS (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C4256A-80		GM71C4256A-10		GM71C4256A-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{REF}	Refresh Period (512 cycle)	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to Write Delay Time	55	-	60	-	70	-	ns	12
t_{RWD}	$\overline{RAS}$ to Write Delay Time	110	-	135	-	160	-	ns	12
t_{AWD}	Column Address to Write Delay	70	-	80	-	95	-	ns	12
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	-	30	ns	
t_{OEZ}	Output buffer trun off Delay Time from $\overline{OE}$	0	20	0	25	0	30 -	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	-	25		30	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ Before $\overline{RAS}$ Refresh	20	-	20		25	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	-	25	-	30	-	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	-	25	-	30	-	ns	

Notes

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltage are refrenced to V_{SS}
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μS is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5nS.
7. V_{IH} (min) and V_{IL} (max) are referenced levels for measuring timing of input signals. Also transition times are required between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. tOFF (max) and tOEZ (max) defines the time at which the output achieves the open circuit condition and is not refrenced to output voltage levels.
10. Either tRCH or tRRH must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t WCS, tRWD, tCWD and tAWD are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min) the cycle is early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle: If tRWD ≥ tRWD(min), tCWD ≥ tCWD(min) and tAWD ≥ tAWD(min) the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a referenced point only: If tRCD is greater than the specified tRCD(max) limit, then access time is controlled by tCAC.
14. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a referenced point only: If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

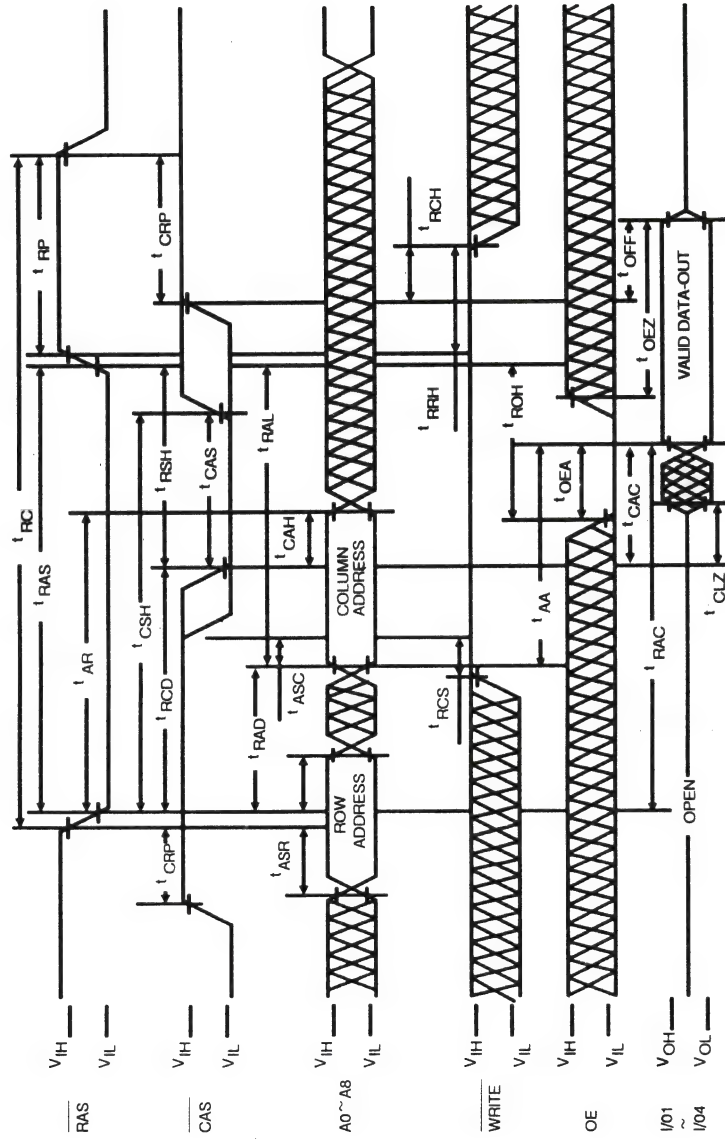


FIGURE 2. READ CYCLE

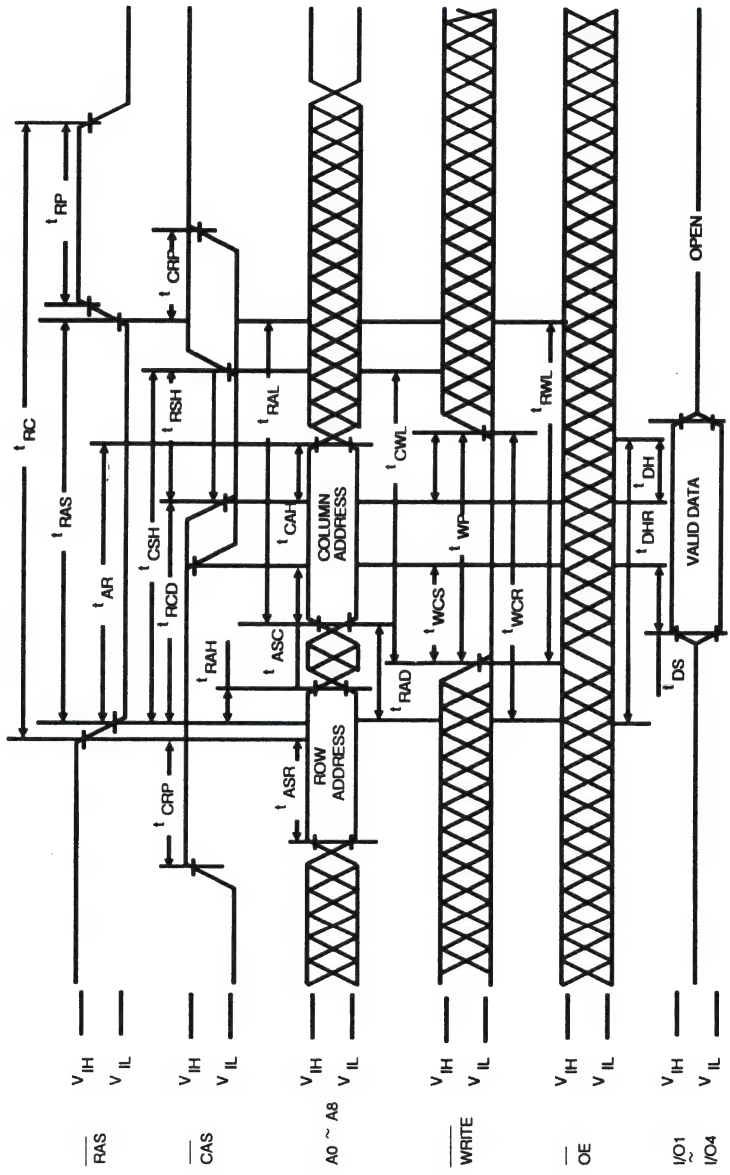


FIGURE 3. WRITE CYCLE (EARLY WRITE)

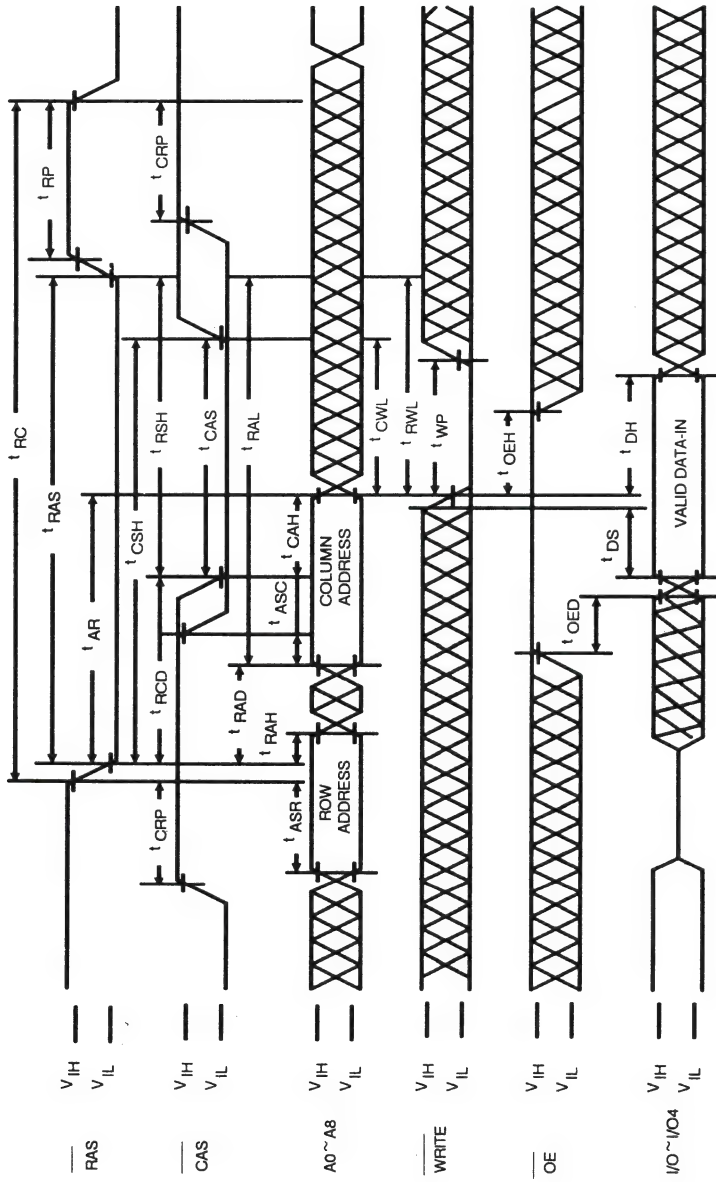


FIGURE 4. WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

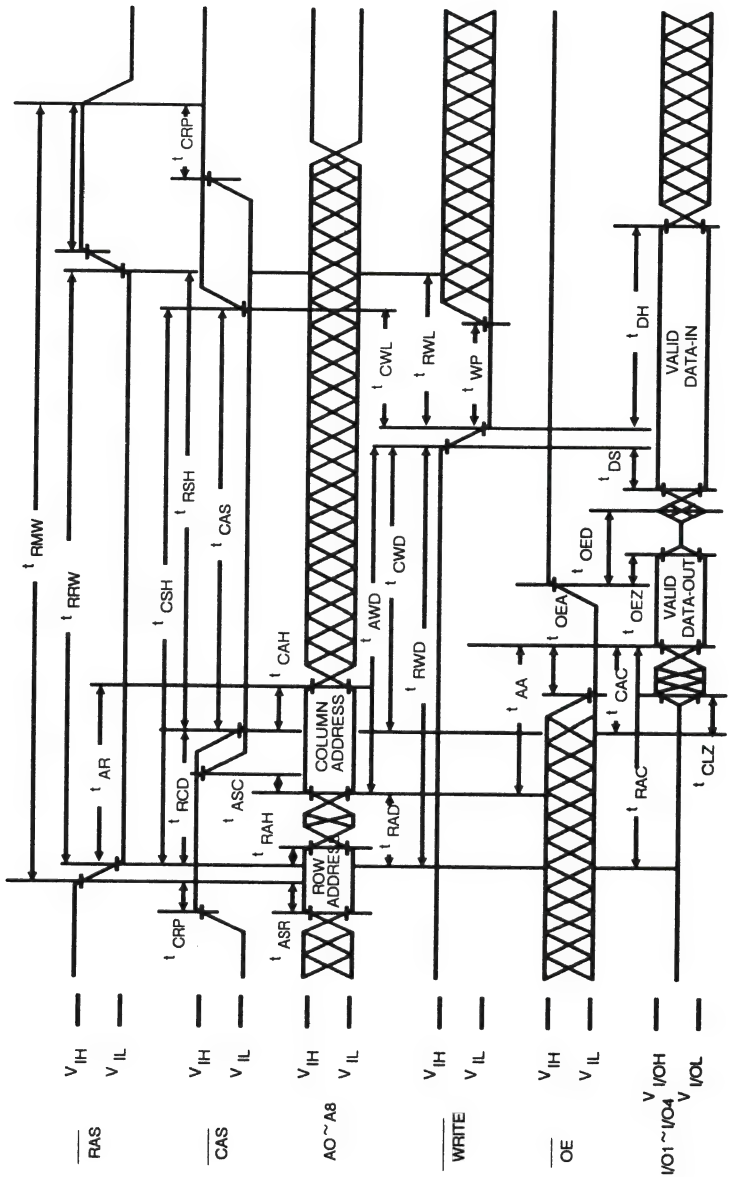


FIGURE 5. READ-MODIFY-WRITE CYCLE

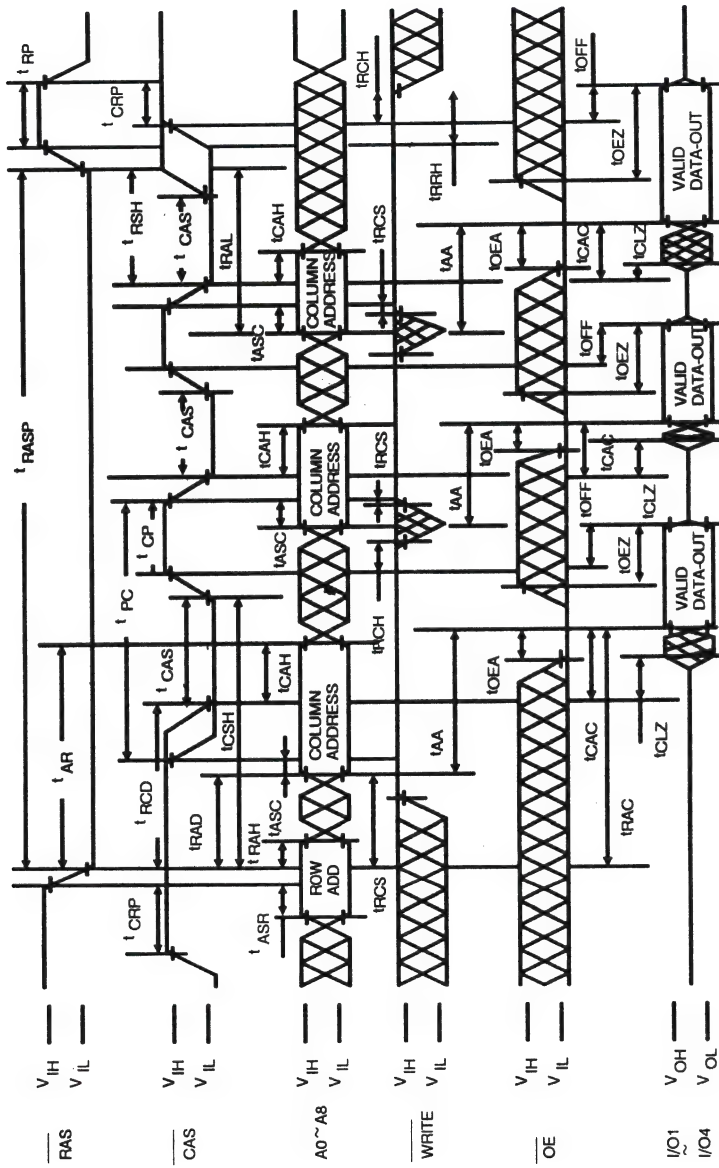


FIGURE 6. FAST PAGE MODE READ CYCLE

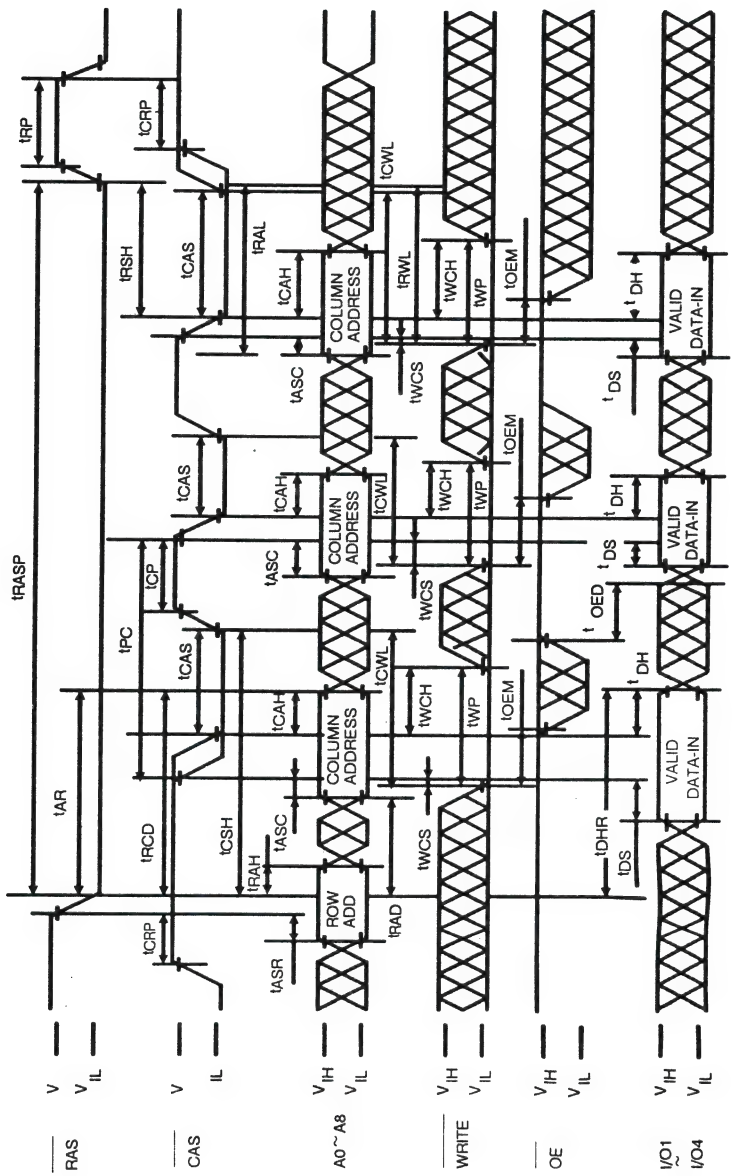


FIGURE 7. FAST PAGE MODE WRITE CYCLE

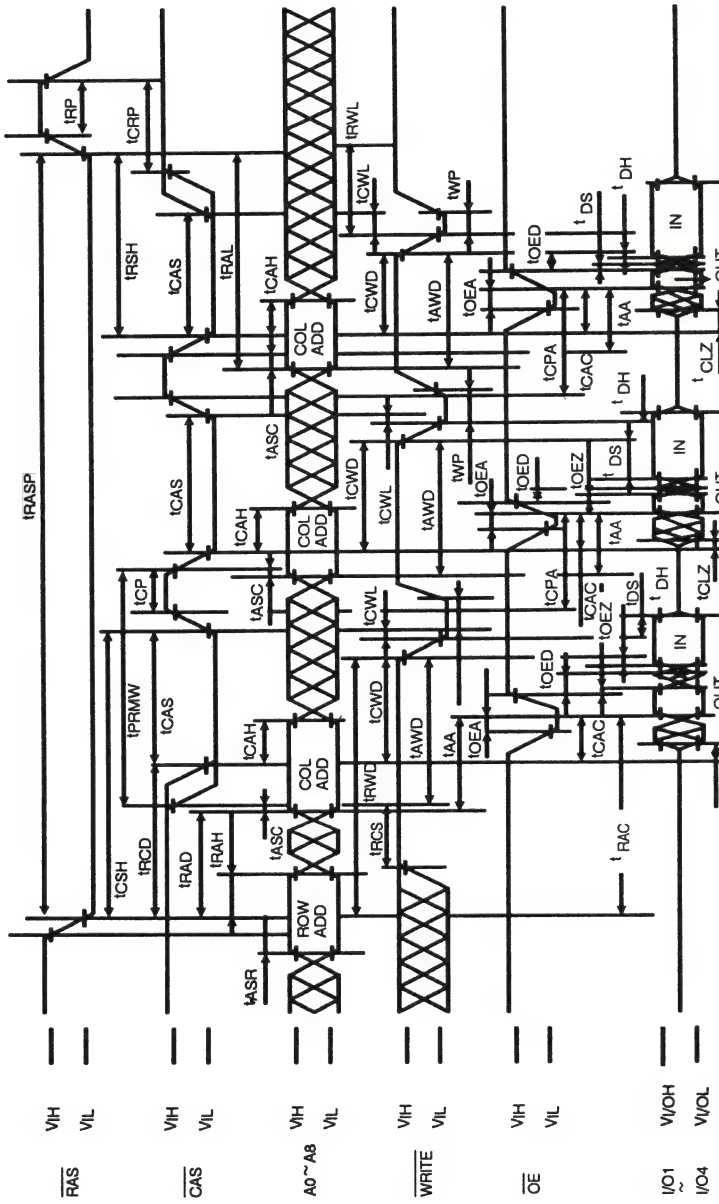


FIGURE 8. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

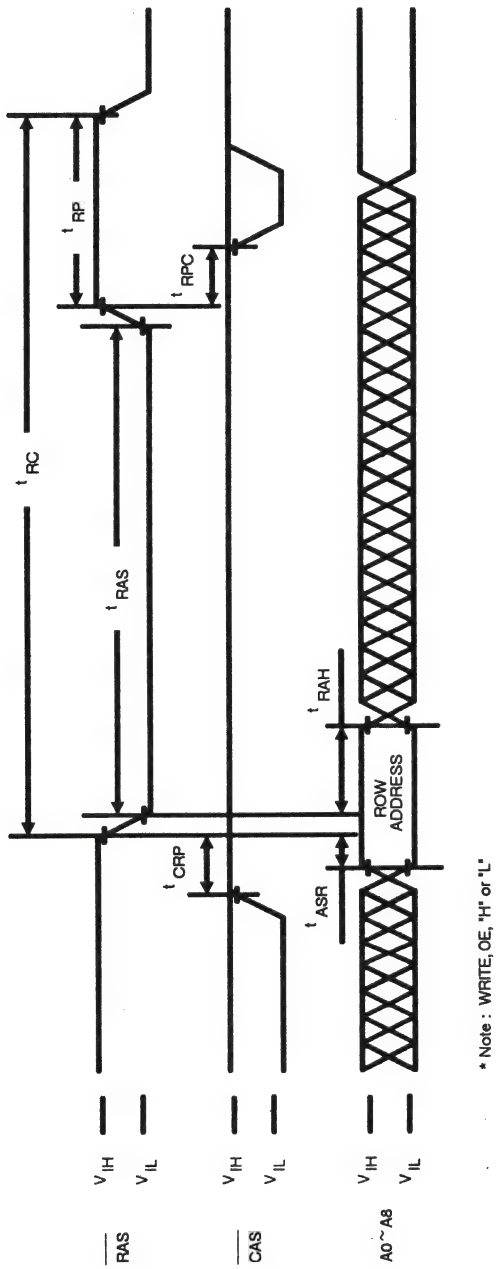
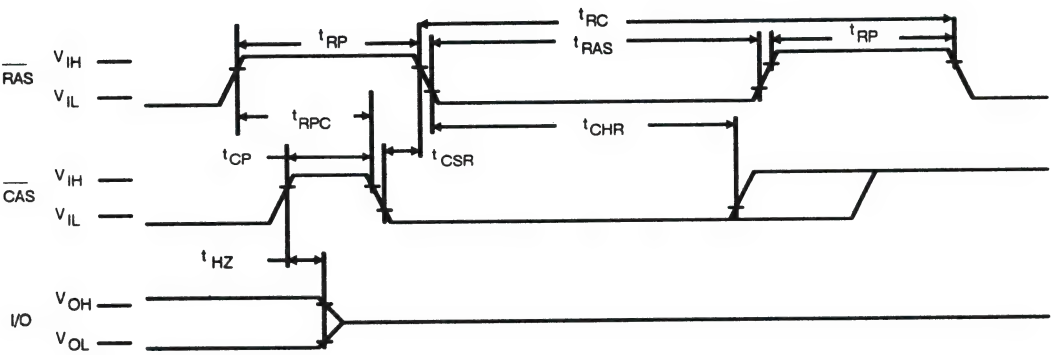


FIGURE 9. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

FIGURE 10. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A0 ~ A7 = Don't care.

FIGURE 11. HIDDEN REFRESH CYCLE (READ)

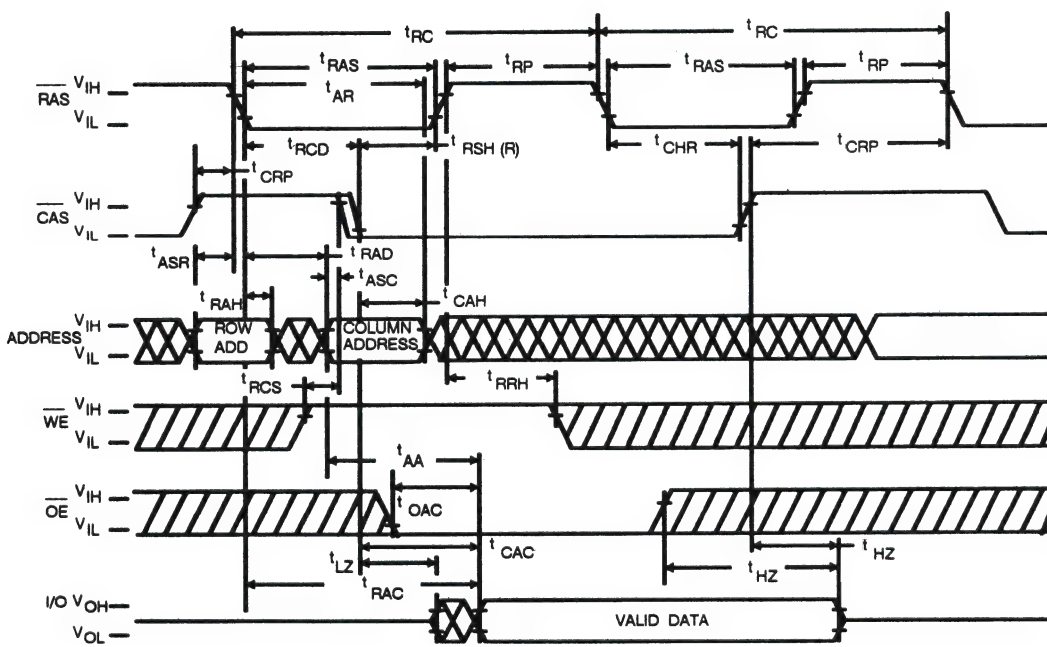


FIGURE 12. HIDDEN REFRESH CYCLE (WRITE)

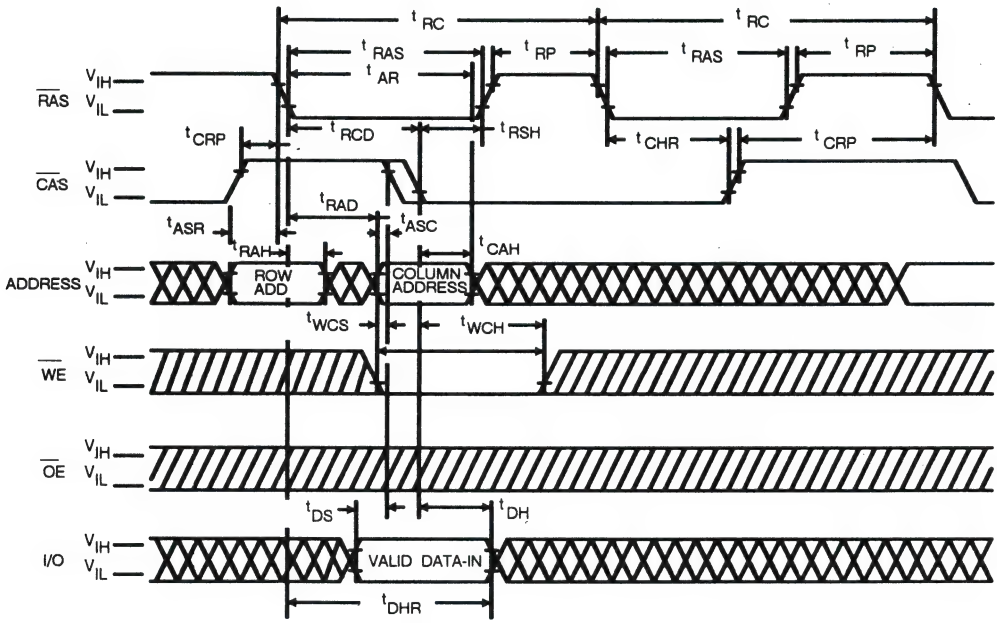
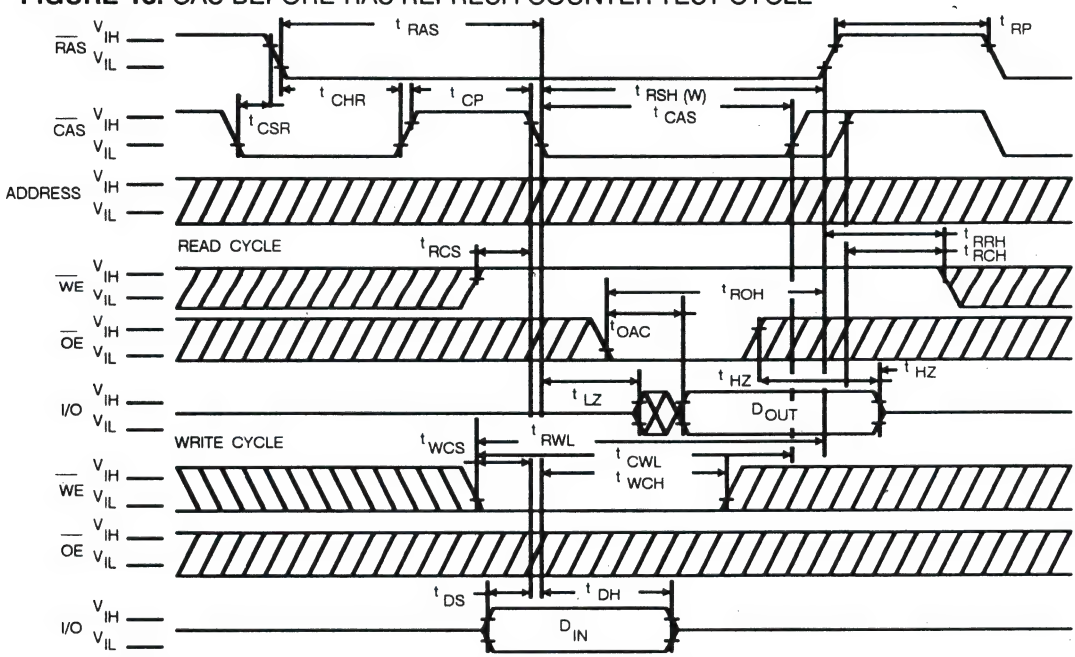
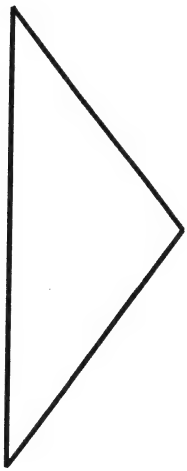


FIGURE 13. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE





PRELIMINARY SPECIFICATION

GM53C461

64K x 4 MULTIPORT VIDEO RAM

Description

The GM53C461 is a high speed 65,536 x 4 bit multiport CMOS dynamic memory. The two ports, random access and serial access, are configured to offer optimum flexibillty in graphics and other systems that require an interface between a processor and a high speed serial data channel such as a CRT or graphics display device.

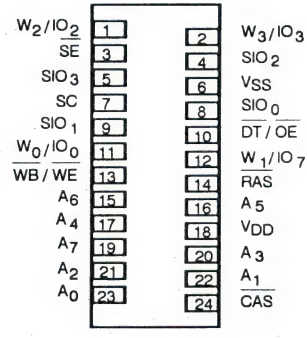
The organization of the random access port of the GM53C461 is exactly like tha GM71C464, a 64K x 4 CMOS DRAM. Additional functions such as transfer between RAM and SAM utillze otherwise unused states of the $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ signals sampled at the falling edge of $\overline{RAS}$ at the beginning of a cycle.

The Serial Access Memory (SAM) is organized as 256 x 4 bits that can be read or written at high speed. The contents of the SAM can be loaded into RAM, and the contents of a selected RAM row (256 x 4) can be loaded into SAM. Except when transferring data between one another, the SAM and RAM operate in an asynchronous manner. The transfer from RAM to SAM or SAM to RAM also refreshes the transferred row in the RAM.

In a RAM to SAM load cycle, 8 bits are needed to specify which of the 256 rows is to be transferred. The state of the address lines at the falling edge of $\overline{CAS}$ is used to specify the starting point in the SAM where data is to be written or read. The static mechanization of the SAM (allowed by CMOS) does not require refreshing. The first access to SAM, either read or write, will be to the location specified at $\overline{CAS}$ time in the previous cycle, and subsequent accesses will continue in an increasing address direction, modulo 256.

24 LEAD PLASTIC ZIP
PIN CONFIGURATION

TOP VLEW



Features

- Dual Port Accessibility
  RAM : 64K x 4 Bit
  SAM : 256 x 4 Bit
- High Speed Access Time
  RAM : 80/100/120 ns
  SAM : 25/30/35 ns
- Low power dissipation for GM53C461-12
  RAM Port operating alone - 50 mA
  SAM Port operating alone - 35 mA
  RAM/SAM operating together - 85 mA
- Low CMOS standby current - 6 mA
- Fast Page Mode access, $\overline{RAS}$-only refresh, and $\overline{CAS}$-before-$\overline{RAS}$ Refresh capabillity
- Bi-directional data transfer between RAM and SAM with real-time operation.
- Bit-masked Write function on RAM port for additional flexibility.
- 256 Refresh cyctes/4 ms
- Standard package is 24 pin ZIP.

Absolute Maximum Ratings

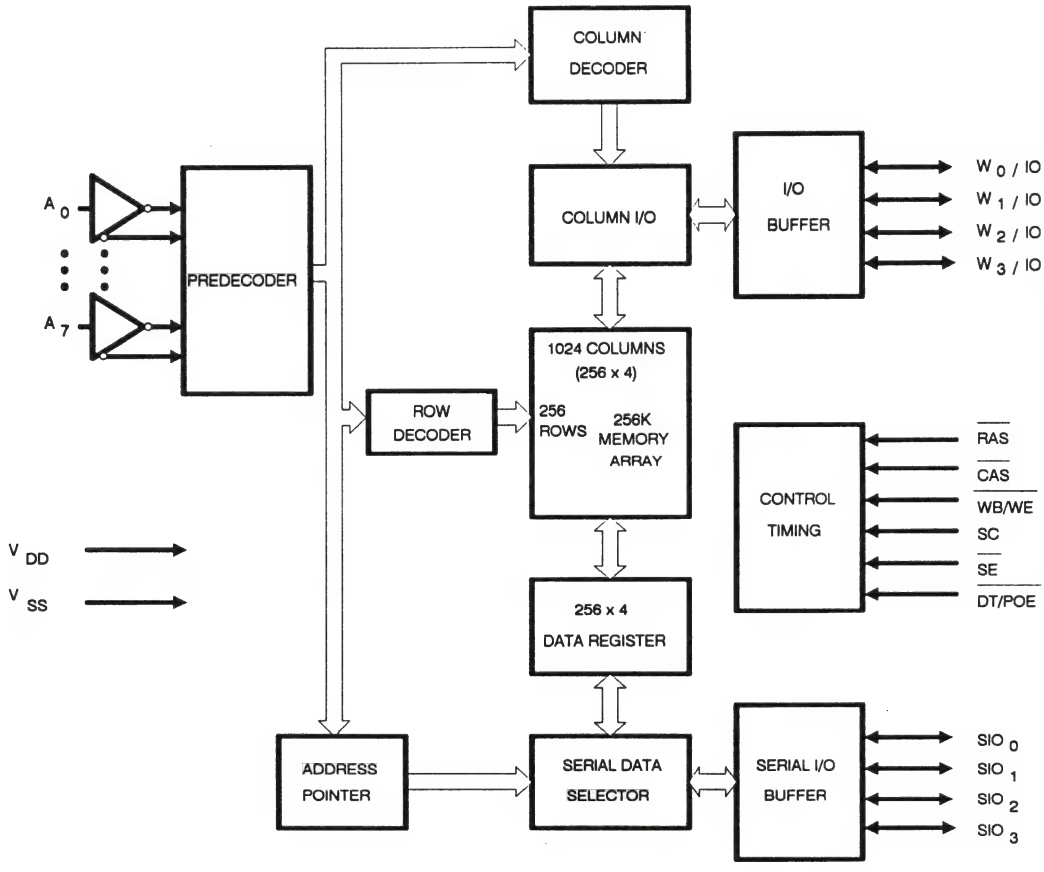
Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature (plastic)	-55°C to +125°C
Voltage on any Pin Excapt V_{DD} Relative to V_{SS}	1.0V to +7.0V
Voltage on V_{DD} relative to V_{SS}	-1.0V to +7.0V
Data Output Current	50mA
Power Dissipation	1.0W

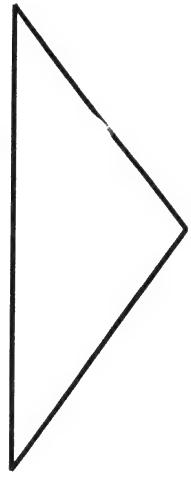
Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions

T_A	Operating Temp.	0 ~ 70°C
V_{CC}	Supply Voltage	4.5 ~ 5.5V
V_{IH}	Input High Voltage	2.4 ~ 6.5V
V_{IL}	Input Low Voltage	-1 ~ 0.8V

Functional Block Diagram





PRODUCT SPECIFICATION

GM231000

131,072 × 8 BITS
STATIC READ ONLY MEMORY

Description

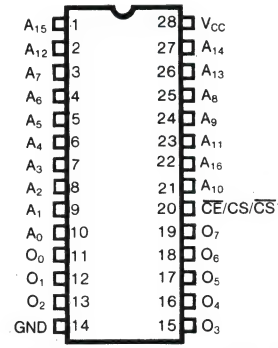
The GM 231000 high-performance Read Only Memory is organized as 131,072 words by eight bits an access time of 250ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important considerations.

The GM231000 offers automatic power down controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH. This feature provides system level power savings of as much as 80%. Pin 20 can also be Mask Programmed as a CS or $\overline{CS}$ allowing two GM231024 ROM's to be wired-OR without external decoding.

This ROM is packaged in industry-standard 28 pin dual-in-line package and is available in ceramic or low-cost plastic.

Pin Configuration

(Top View)

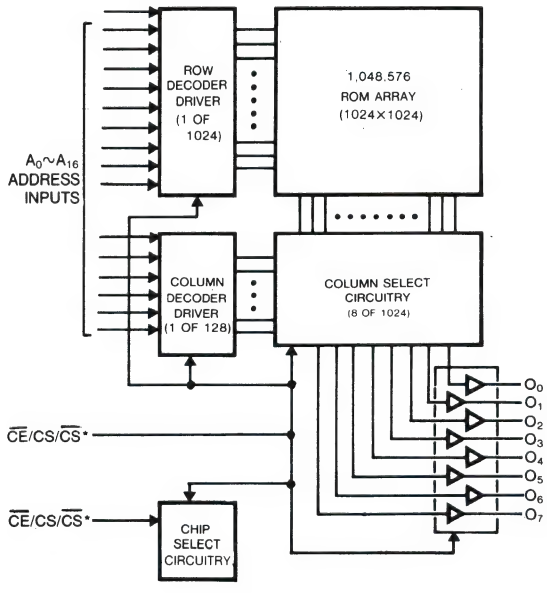


* CHIP SELECT(CS) IS PROGRAMMAGLE ACTIVE LOW OR ACTIVE HIGH.

Feature

- **131,072 × 8 organization**
- **Single +5V Supply**
- **Access time 250ns (max)**
- **Totally static operation**
- **Completely TTL compatible**
- **Operating current 100mA (max)**
- **Standby current 20mA (max)**
- **Automatic power down ($\overline{CE}$)**
  Programmable Chip Select
  3-state outputs for wired-OR expansion
- **28-pin industry-standard DIP**
- **EPROMs accepted as program data input**

Block Diagram



Pin Name

$A_2 \sim A_{16}$	:	Address Input
$O_0 \sim O_7$	:	Data Output
$\overline{CE}$	:	Chip Enable Input
$CS/\overline{CS}$	:	Chip Select Input
V_{CC}	:	Power Supply
GND	:	Ground

Absolute Maximum Ratings

Ambient Operating Temp	V_{amb}	−10 to +80°C
Storage Temp	V_{STG}	−65 to +150°C
Supply Voltage Ground Potential	V_{CC}	−0.5 to +7.0V
Applied Output Voltage	V_{OUT}	−0.5 to +7.0V
Applied Input Voltage	V_{IN}	−0.5 to + 7.0V
Power Dissipation	P_D	1.0W

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: T_A=0°C to + 70°C, V_{CC}=5.0V±10%, V_{SS}=0V

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=−1.0mA	2.4	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA		0.4	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	V
I_{LI}	Input Leakage Current	V_{IN}=0V to V_{CC}		10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0V to V_{CC}		10	μA
I_{CC}	Operating Supply Current	Note 1		100	mA
I_{SB}	Standby Supply Current	$\overline{CE}$=V_{IH}		20	mA
I_{OS}	Output Short Circuit Current	Note 2		90	mA

AC Operating Characteristics: T_A=0° to+70°C, V_{CC}=+5V±10%

SYMBOL	PARAMETER	GM231000-25		UNIT	NOTES
		MIN	MAX		
t_{CYC}	Cycle Time	250		ns	
t_{AA}	Address Access Time		250	ns	
t_{OH}	Output Hold After Address Change	10		ns	
t_{ACE}	Chip Enable Access Time		250	ns	
t_{ACS}	Chip Select Access Time		100	ns	
t_{LZ}	Output LOW Z Delay	10		ns	3
t_{HZ}	Output HIGH Z Delay		100	ns	4

Capacitance: T_A = 25°C, f = 1.0 MHz, Note 5

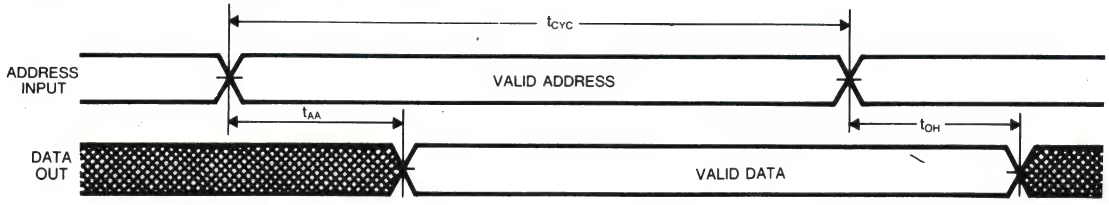
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_I	Input Capacitance	V_{IN}=0V		5	pF
C_O	Output Capacitance	V_{OUT}=0V		5	pF

Notes:

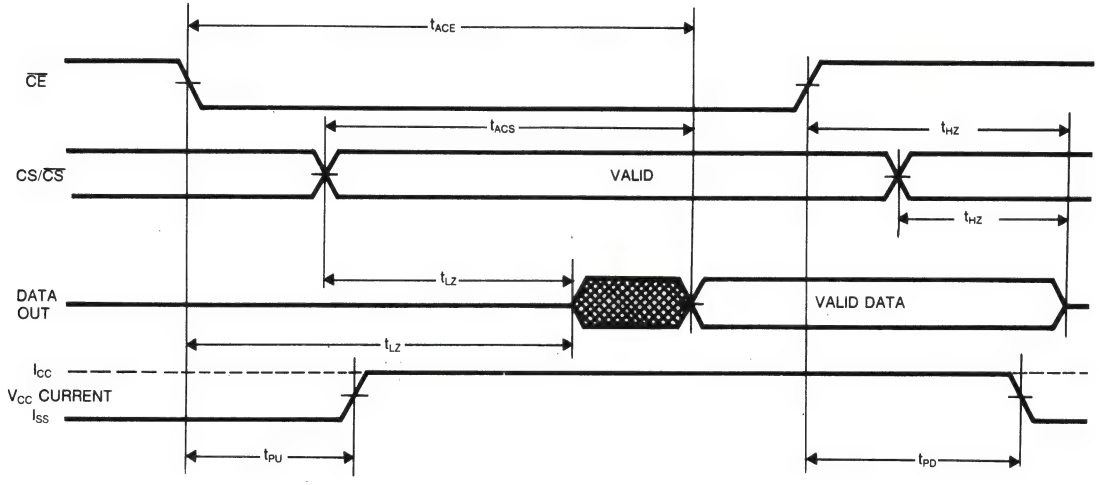
1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. Output LOW impedance delay (TLZ) is measured from $\overline{CE}$ or CS going active.
4. Output HIGH impedance delay (THZ) is measured from $\overline{CE}$ or CS going inactive.
5. This parameter is periodically sampled and is not 100% tested.

Timing Waveforms

Propagation Delay From Address ($\overline{CE}$/CS/$\overline{CS}$ Active)



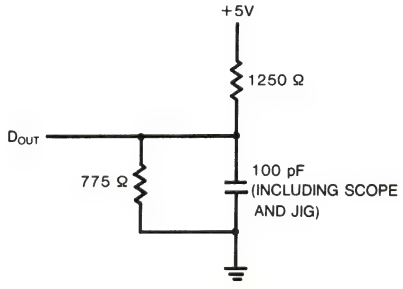
Propagation Delay From Chip Enable, Chip Select or Output Enable (Address Valid)



AC Test Conditions

Input Pulse Levels	0.8 to 2.2V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8 and 2.0V
Output Load	See Figure 1

FIGURE 1



PRODUCT SPECIFICATION

GM231000-30A,31A,32A

16 x 16 DOT MATRIX SPECIAL KOREAN & CHINESE CHARACTER GENERATOR ROMS

Description

The GM231000-30A, 31A and 32A are standard SPECIAL, KOREAN & CHINESE character generator ROMs. Each device is Organized as 131, 072 words by eight bits with on access time of 250 ns.
They include 8,224 character sets of 16 by 16 dot matrix per a character (986 special characters, 2,350 KOREAN characters, 4,888 CHINESE characters, PC256 characters, and 6 user defined KOREAN character sets.)

Features

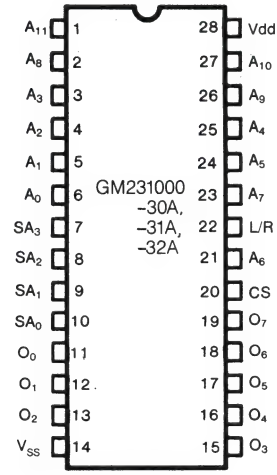
- **Include 8,224 standard SPECIAL, KOREAN & CHINESE character sets.**
- **PC 256 characters are ordered in two ways. (8×16 dot matrix display)**
- **16 x 16 dot matrix display**
- **Row scan display**
- **High speed access time : 250ns Max.**
- **Suitable for CRT display**
- **Completely TTL compatible**
- **3 state output**
- **Single +5V power supply**
- **N channel MOSFET**

Pin Name

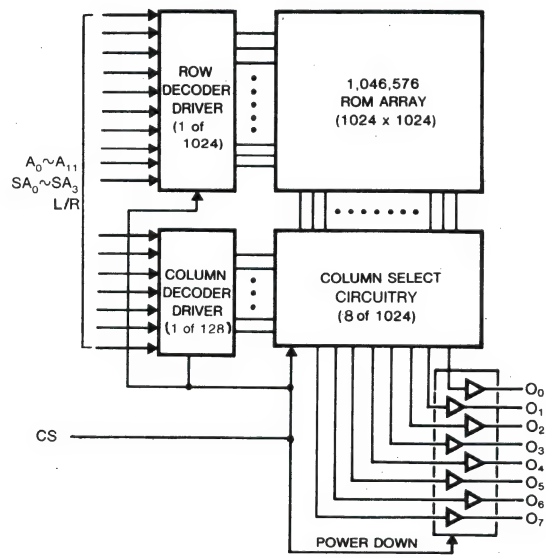
$SA_0 \sim SA_4$	:	Scan address inputs
$\overline{L}/R$	:	Left right plane selector
$A_0 \sim A_{11}$	:	Character address inputs
$\overline{CS}$	:	Chip select input (Active low)
$O_0 \sim O_7$	:	Data outputs
Vdd	:	+5V power supply
V_{SS}	:	Ground

Pin Configuration

(Top View)



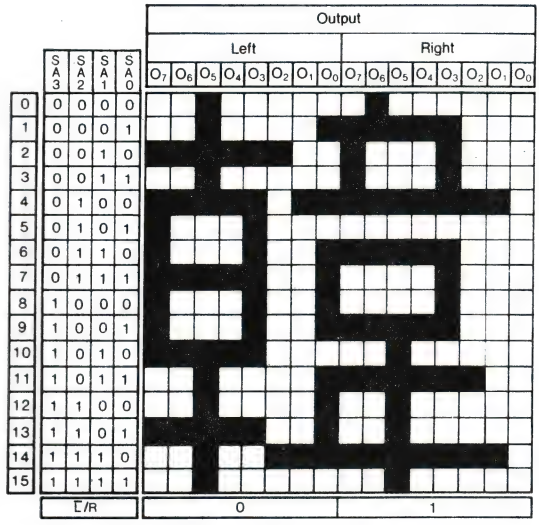
Block Diagram



Pin Description

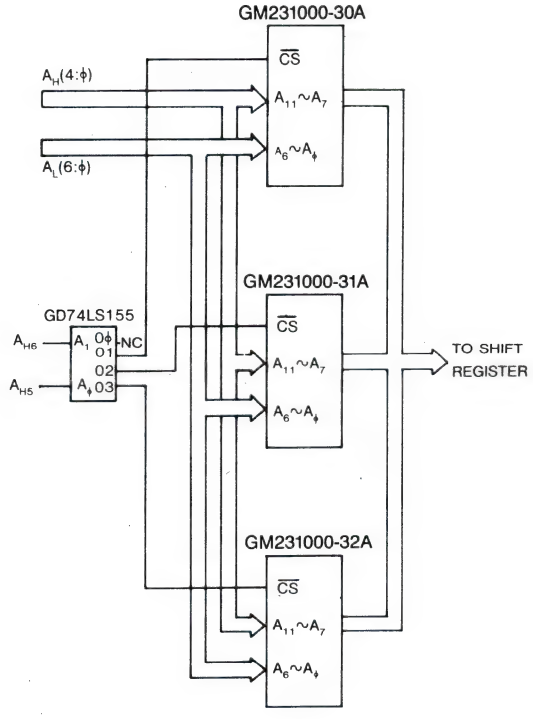
- $SA_0 \sim SA_3$: Scan Address Input
  $SA_0 \sim SA_3$ are 4 bit address Input from CRTC for displaying a line of rows.
- $\overline{L}/R$: Left/Right plane selector
  Appoint a left or a right plane
- $A_0 \sim A_{11}$: Character Address Input
  $A_0 \sim A_{11}$ form 12 bit address input, appoint 4,096 Chinese Character sets.
- $O_0 \sim O_7$: Data Output
  Transfer 8 bit data for displaying dot matrix. The "1" displays a dot, the "0" displays a space. If the $\overline{CS}$ is high, $O_0 \sim O_7$ are in High-impedance state.
- $\overline{CS}$: Chip Select Input (active low)
  If the $\overline{CS}$ is high then the ROM will be in low power standby mode operating.
- Vdd: +5V Power Supply
- Vss: Ground.

Character Pattern Architecture



Note: ■ Output Data "1"
□ Output Data "0"

Typical Application



Absolute Maximum Ratings

Ambient Operating Temperature	T_{amb}	−10 to +80°C
Storage Temperature	T_{STG}	−65 to +150°C
Supply Voltage to Ground Potential	V_{dd}	−0.5 to +7.0V
Applied Output Voltage	V_{OUT}	−0.5 to +7.0V
Applied Input Voltage	V_{IN}	−0.5 to +7.0V
Power Dissipation	P_D	1.0W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics; T_A=0° to +70°C, V_{CC}=+5V ± 10%

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=−1.0mA	2.4	V_{dd}	V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA		0.4	V
V_{IH}	Input High Voltage		2.0	V_{dd}	V
V_{IL}	Input Low Voltage		−0.5	0.8	V
I_{LI}	Input Leakage Current	V_{IN}=0V to V_{dd}		10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0V to V_{dd}		10	μA
I_{dd}	Operating Supply Current	Note 1		100	mA
I_{OS}	Output Short Circuit Current	Note 2		70	mA

AC Operating Characteristics; T_A=0° to +70°C, V_{dd}=+5V ± 10%

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CYC}	Cycle Time	250		ns	
t_{AA}	Address Access Time		250	ns	
t_{OH}	Output Hold After Address Change	10		ns	
t_{ACS}	Chip Select Access Time		250	ns	
t_{LZ}	Output Low Z Delay	10		ns	3
t_{HZ}	Output High Z Delay		100	ns	4

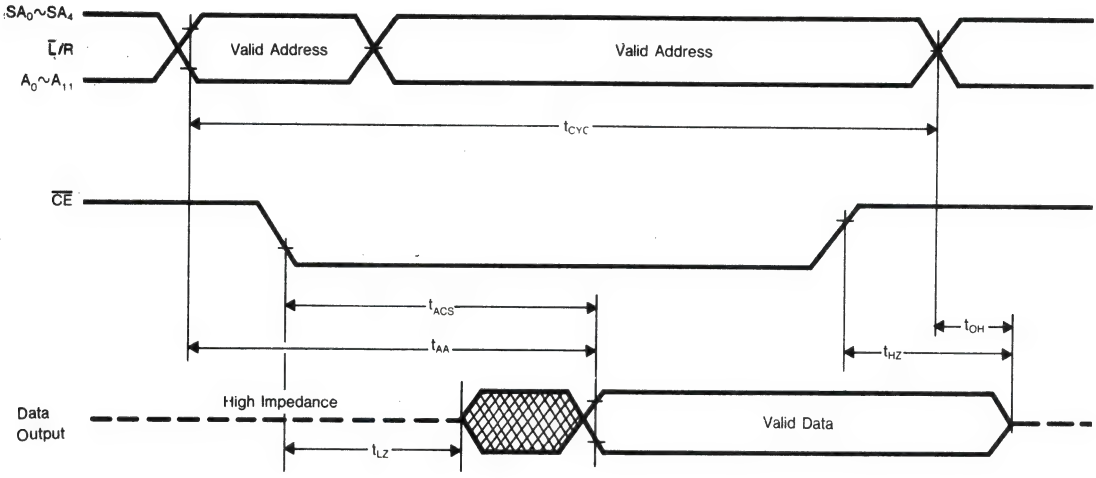
Notes

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. Output low impedance delay (TLZ) is measured from $\overline{CE}$ going active.
4. Output high impedance delay (THZ) is measured from $\overline{CE}$ going inactive.
5. This parameter is periodically sampled and is not 100% tested.

Capacitance T_A=25°C, f=1.0 MHz, Note 5

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_I	Input Capacitance	V_{IN}=0 V		5	pF
C_O	Output Capacitance	V_{OUT}=0 V		5	pF

Timing Waveforms



AC Test Condition

Input Pulse Levels	0.8 to 2.2V
Input Rise and Fall Times	10 ns
Input Timing Level	1.5 V
Output Timing Level	0.8 and 2.0 V
Output Load	See Figure 1

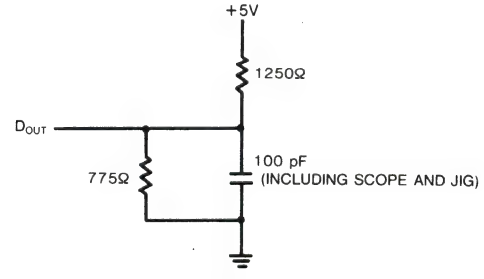
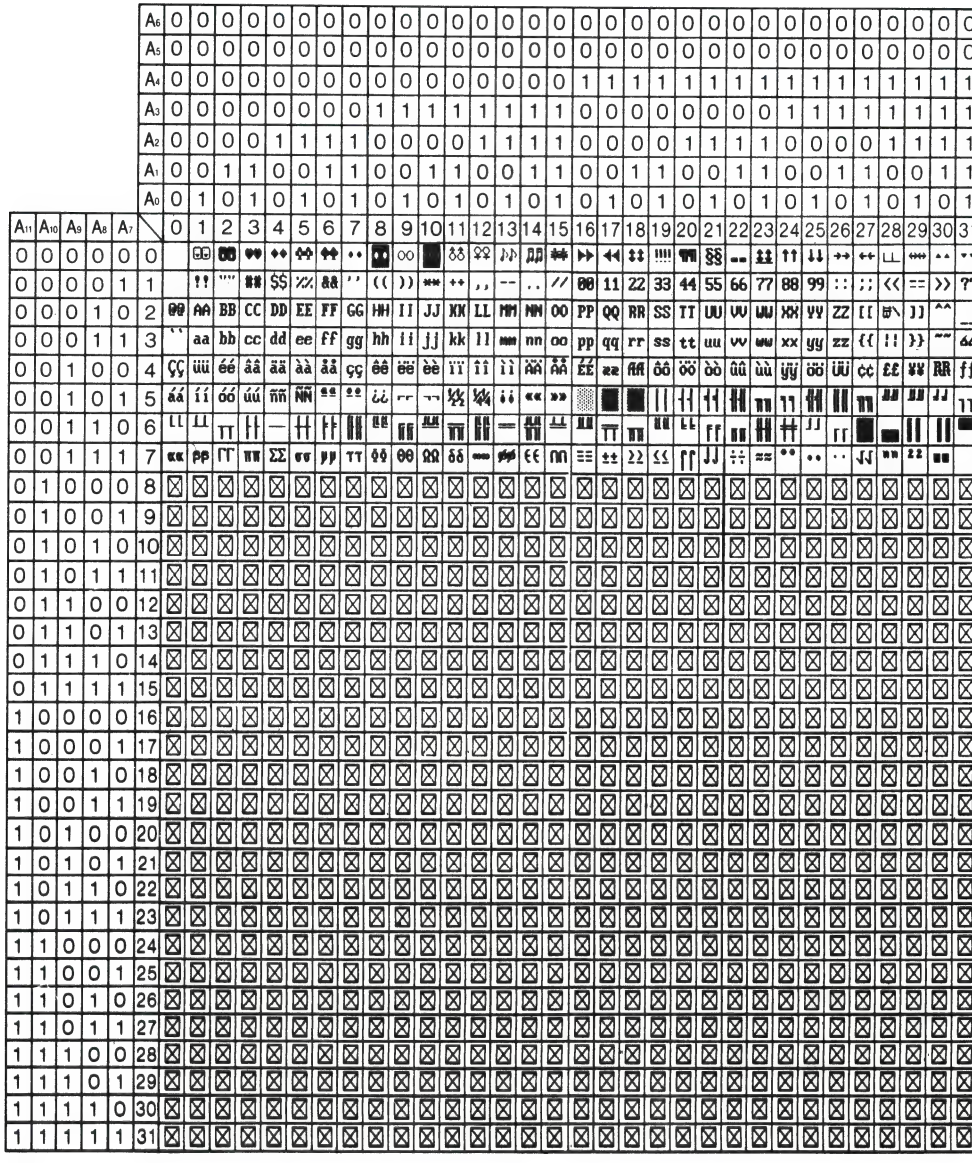


Fig. 1

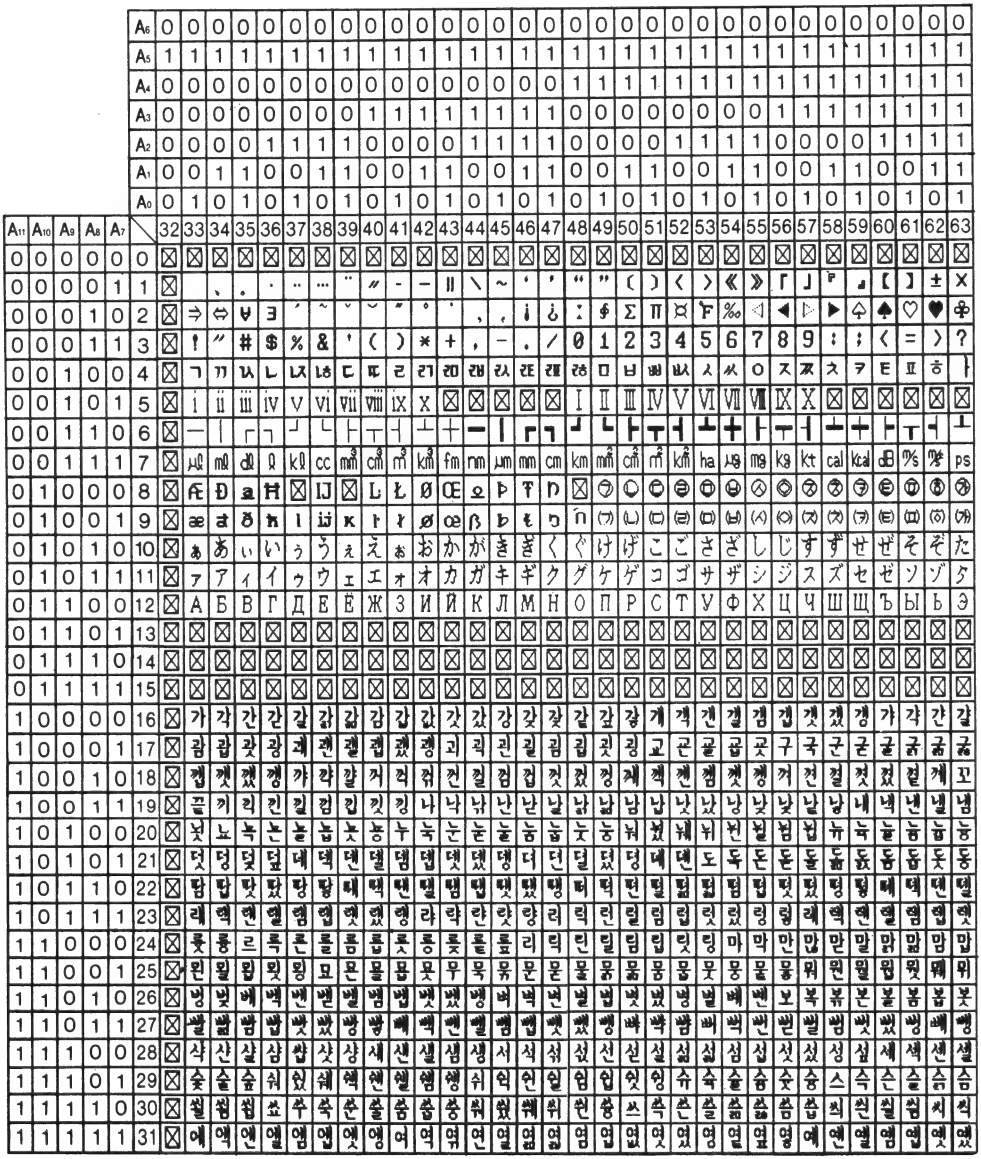
Memory Allocation for SPECIAL KOREAN & CHINESE 1Mb Mask ROM

30A-1	30A-2	30A-3	30A-4
31A-1	31A-2	31A-3	31A-4
32A-1	32A-2	32A-3	32A-4

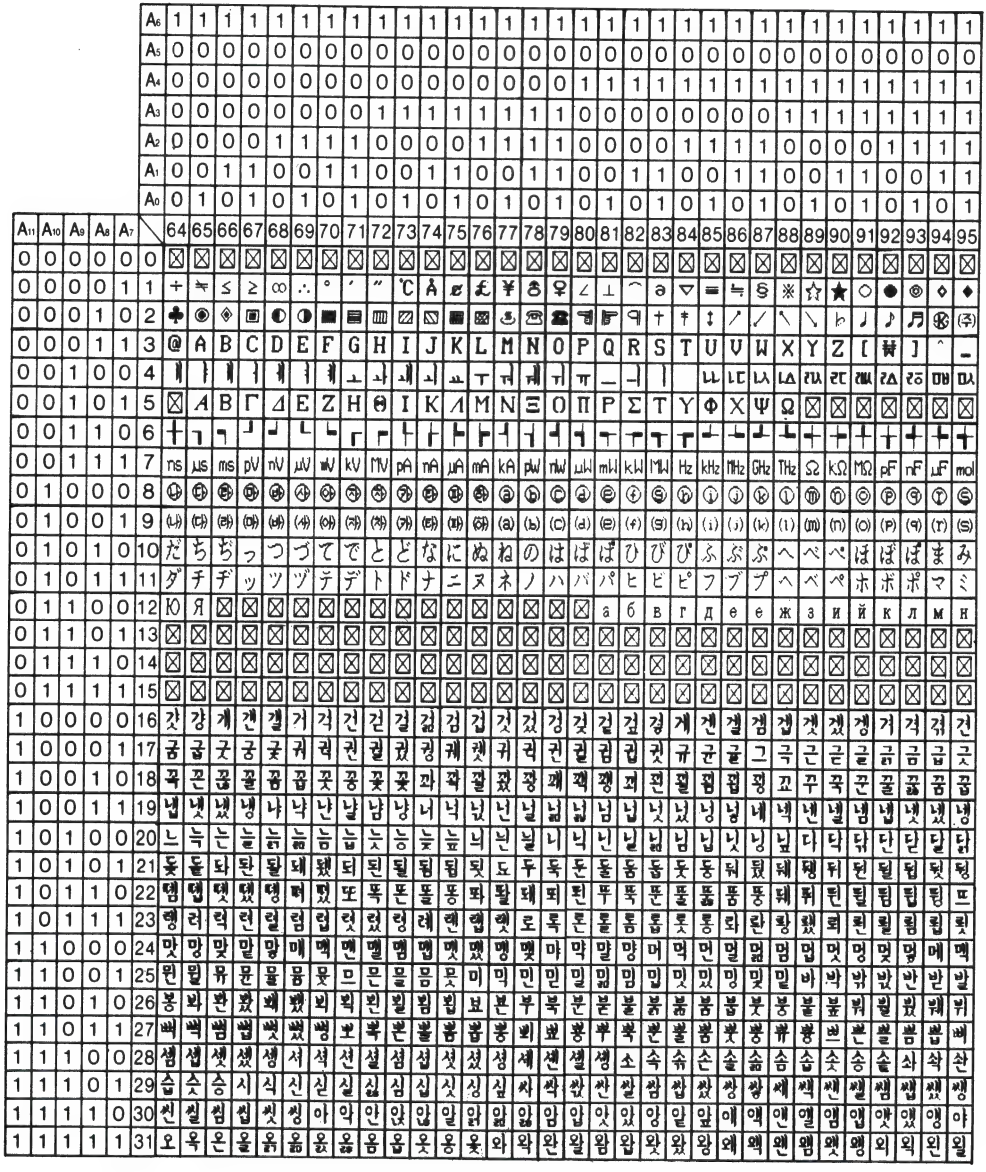
Character Allocation Table: 30A-1



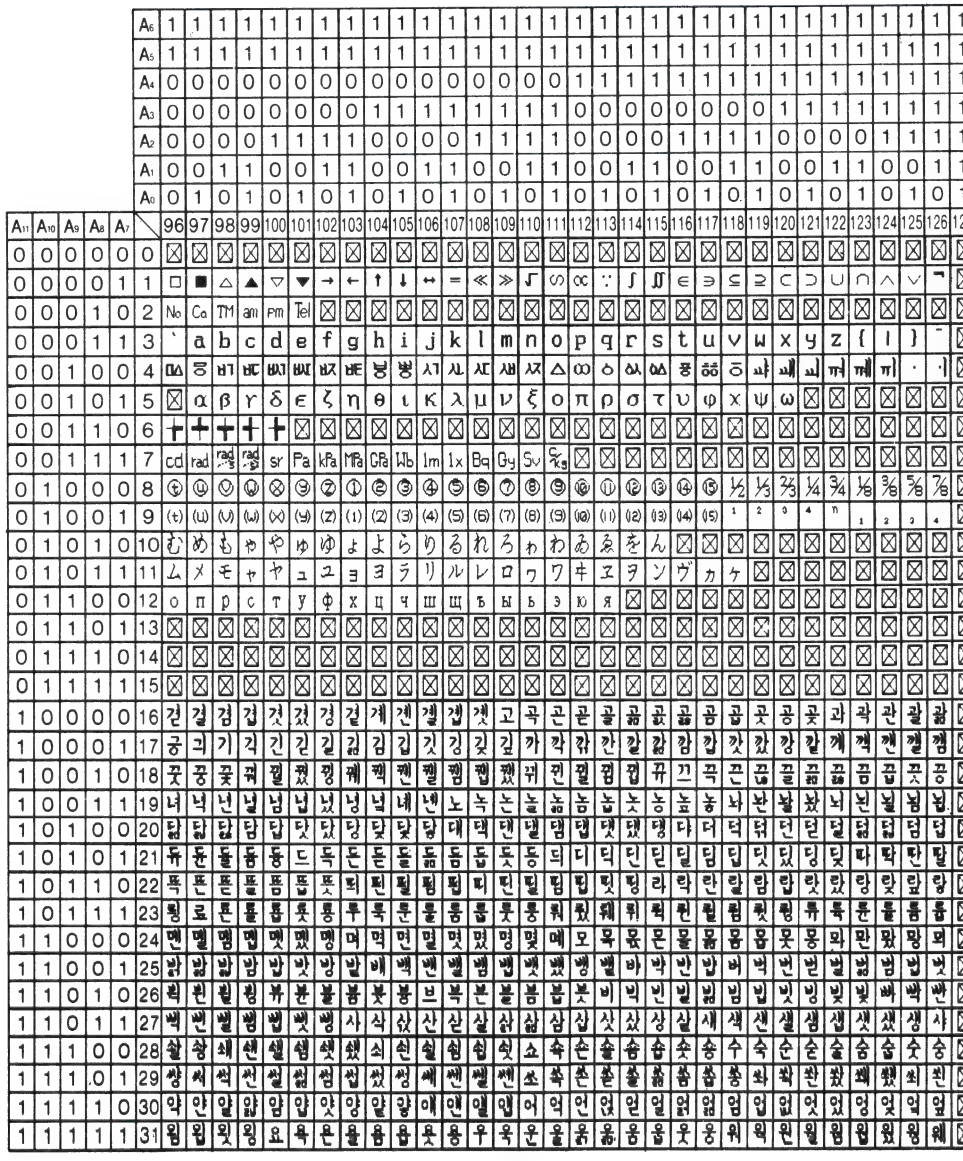
Character Allocation Table: 30A-2



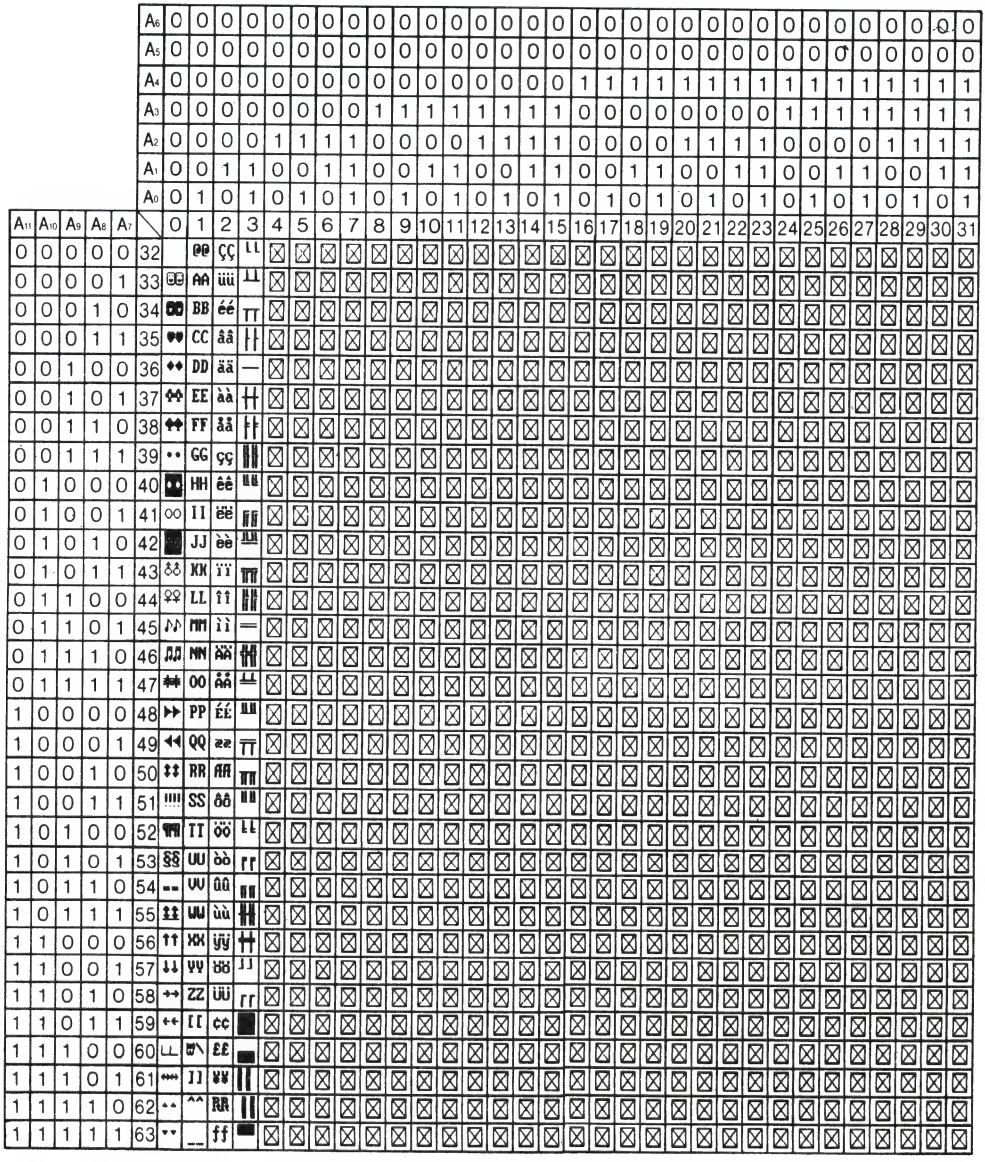
Character Allocation Table: 30A-3



Character Allocation Table: 30A-4



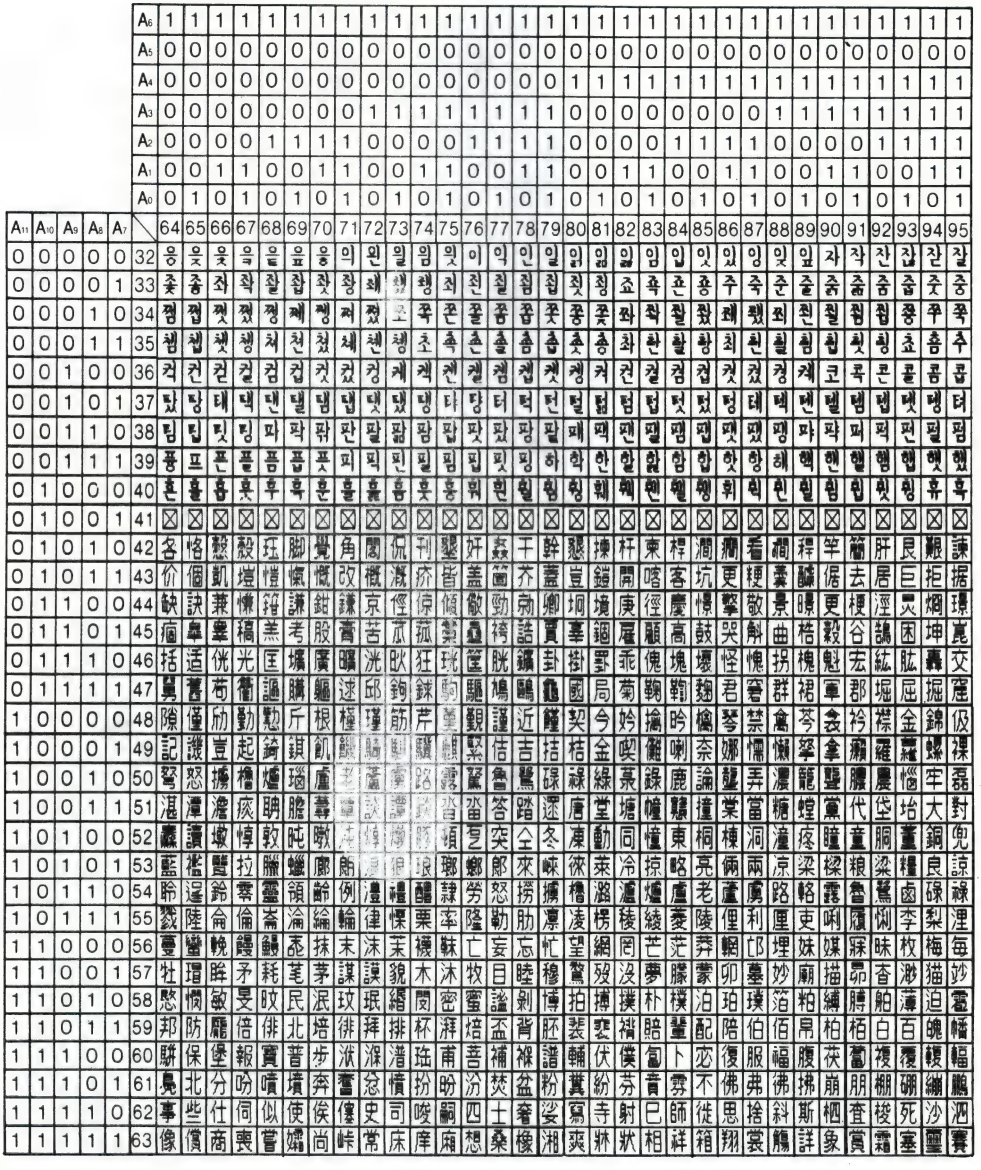
Character Allocation Table: 31A-1



Character Allocation Table: 31A-2

					A6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					A5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A11	A10	A9	A8	A7		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
0	0	0	0	0	32	☒	웩	웬	웰	웸	웹	웽	위	윅	윈	윌	윔	윕	윗	윙	유	육	윤	율	윰	윱	윳	융	윷	으	윽	은	을	읊	음	읍	읏
0	0	0	0	1	33	☒	점	접	젓	정	젖	제	젝	젠	젤	젬	젭	젯	젱	져	젼	졀	졈	졉	졌	졍	졔	조	족	존	졸	졺	좀	좁	좃	종	좆
0	0	0	1	0	34	☒	징	짖	짙	짚	짜	짝	짠	짢	짤	짧	짬	짭	짯	짰	짱	째	짹	짼	쨀	쨈	쨉	쨋	쨌	쨍	쨔	쨘	쨩	쩌	쩍	쩐	쩔
0	0	0	1	1	35	☒	찼	창	찾	채	책	챈	챌	챔	챕	챗	챘	챙	챠	챤	챦	챨	챰	챵	처	척	천	철	첨	첩	첫	첬	청	체	첵	첸	첼
0	0	1	0	0	36	☒	치	칙	친	칟	칠	칡	침	칩	칫	칭	카	칵	칸	칼	캄	캅	캇	캉	캐	캑	캔	캘	캠	캡	캣	캤	캥	캬	캭	컁	커
0	0	1	0	1	37	☒	큄	큅	큇	큉	큐	큔	큘	큠	크	큭	큰	클	큼	큽	킁	키	킥	킨	킬	킴	킵	킷	킹	타	탁	탄	탈	탉	탐	탑	탓
0	0	1	1	0	38	☒	퉤	튀	튁	튄	튈	튐	튑	튕	튜	튠	튤	튬	튱	트	특	튼	튿	틀	틂	틈	틉	틋	틔	틘	틜	틤	틥	티	틱	틴	틸
0	0	1	1	1	39	☒	퐈	퐝	푀	푄	표	푠	푤	푭	푯	푸	푹	푼	푿	풀	풂	품	풉	풋	풍	풔	풩	퓌	퓐	퓔	퓜	퓟	퓨	퓬	퓰	퓸	퓻
0	1	0	0	0	40	☒	혤	혭	호	혹	혼	홀	홅	홈	홉	홋	홍	홑	화	확	환	활	홧	황	홰	홱	홴	횃	횅	회	획	횐	횔	횝	횟	횡	효
0	1	0	0	1	41	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒
0	1	0	1	0	42	☒	伽	佳	假	價	加	可	呵	哥	嘉	嫁	家	暇	架	枷	柯	歌	珂	痂	稼	苛	茄	街	袈	訶	賈	跏	軻	迦	駕	刻	却
0	1	0	1	1	43	☒	匣	岬	甲	胛	鉀	閘	剛	堈	姜	岡	崗	康	強	彊	慷	江	畺	疆	糠	絳	綱	羌	腔	舡	薑	襁	講	鋼	降	鱇	介
0	1	1	0	0	44	☒	瞼	鈐	黔	劫	怯	迲	偈	憩	揭	擊	格	檄	激	膈	覡	隔	堅	牽	犬	甄	絹	繭	肩	見	譴	遣	鵑	抉	決	潔	結
0	1	1	0	1	45	☒	棨	溪	界	癸	磎	稽	系	繫	繼	計	誡	谿	階	鷄	古	叩	告	呱	固	姑	孤	尻	庫	拷	攷	故	敲	暠	枯	槁	沽
0	1	1	1	0	46	☒	科	菓	誇	課	跨	過	鍋	顆	廓	槨	藿	郭	串	冠	官	寬	慣	棺	款	灌	琯	瓘	管	罐	菅	觀	貫	關	館	刮	恝
0	1	1	1	1	47	☒	區	口	句	咎	嘔	坵	垢	寇	嶇	廐	懼	拘	救	枸	柩	構	歐	毆	毬	求	溝	灸	狗	玖	球	瞿	矩	究	絿	耉	臼
1	0	0	0	0	48	☒	鬼	龜	叫	圭	奎	揆	槻	珪	硅	窺	竅	糾	葵	規	赳	逵	閨	勻	均	畇	筠	菌	鈞	龜	橘	克	剋	劇	戟	棘	極
1	0	0	0	1	49	☒	朞	期	杞	棋	棄	機	欺	氣	汽	沂	淇	玘	琦	琪	璂	璣	畸	畿	碁	磯	祁	祇	祈	祺	箕	紀	綺	羈	耆	耭	肌
1	0	0	1	0	50	☒	納	臘	蠟	衲	囊	娘	廊	朗	浪	狼	郎	乃	來	內	奈	柰	耐	冷	女	年	撚	秊	念	恬	拈	捻	寧	寗	努	勞	奴
1	0	0	1	1	51	☒	丹	亶	但	單	團	壇	彖	斷	旦	檀	段	湍	短	端	簞	緞	蛋	袒	鄲	鍛	撻	澾	獺	疸	達	啖	坍	憺	擔	曇	淡
1	0	1	0	0	52	☒	棹	櫂	淘	渡	滔	濤	燾	盜	睹	禱	稻	萄	覩	賭	跳	蹈	逃	途	道	都	鍍	陶	韜	毒	瀆	牘	犢	獨	督	禿	篤
1	0	1	0	1	53	☒	蘿	螺	裸	邏	樂	洛	烙	珞	絡	落	諾	酪	駱	丹	亂	卵	欄	欒	瀾	爛	蘭	鸞	剌	辣	嵐	擥	攬	欖	濫	籃	纜
1	0	1	1	0	54	☒	煉	璉	練	聯	蓮	輦	連	鍊	冽	列	劣	洌	烈	裂	廉	斂	殮	濂	簾	獵	令	伶	囹	寧	岺	嶺	怜	玲	笭	羚	翎
1	0	1	1	1	55	☒	遼	鬧	龍	壘	婁	屢	樓	淚	漏	瘻	累	縷	蔞	褸	鏤	陋	劉	旒	柳	榴	流	溜	瀏	琉	瑠	留	瘤	硫	謬	類	六
1	1	0	0	0	56	☒	立	笠	粒	摩	瑪	痲	碼	磨	馬	魔	麻	寞	幕	漠	膜	莫	邈	万	卍	娩	巒	彎	慢	挽	晩	曼	滿	漫	灣	瞞	萬
1	1	0	0	1	57	☒	蔑	冥	名	命	明	暝	椧	溟	皿	瞑	茗	蓂	螟	酩	銘	鳴	袂	侮	冒	募	姆	帽	慕	摸	摹	暮	某	模	母	毛	牟
1	1	0	1	0	58	☒	汶	紊	紋	聞	蚊	門	雯	勿	沕	物	味	媚	尾	嵋	彌	微	未	梶	楣	渼	湄	眉	米	美	薇	謎	迷	靡	黴	岷	悶
1	1	0	1	1	59	☒	發	跋	醱	鉢	髮	魃	倣	傍	坊	妨	尨	幇	彷	房	放	方	旁	昉	枋	榜	滂	磅	紡	肪	膀	舫	芳	蒡	蚌	訪	謗
1	1	1	0	0	60	☒	碧	蘗	闢	霹	便	卞	弁	變	辨	辯	邊	別	瞥	鱉	鼈	丙	倂	兵	屛	幷	昞	昺	柄	棅	炳	甁	病	秉	竝	輧	餠
1	1	1	0	1	61	☒	孚	孵	富	府	復	扶	敷	斧	浮	溥	父	符	簿	缶	腐	腑	膚	艀	芙	莩	訃	負	賦	賻	赴	趺	部	釜	阜	附	駙
1	1	1	1	0	62	☒	脾	臂	菲	蜚	裨	誹	譬	費	鄙	非	飛	鼻	嚬	嬪	彬	斌	檳	殯	浜	濱	瀕	牝	玭	貧	賓	頻	憑	氷	聘	騁	乍
1	1	1	1	1	63	☒	傘	刪	山	散	汕	珊	産	疝	算	蒜	酸	霰	乷	撒	殺	煞	薩	三	參	杉	森	滲	芟	蔘	衫	揷	澁	鈒	颯	上	傷

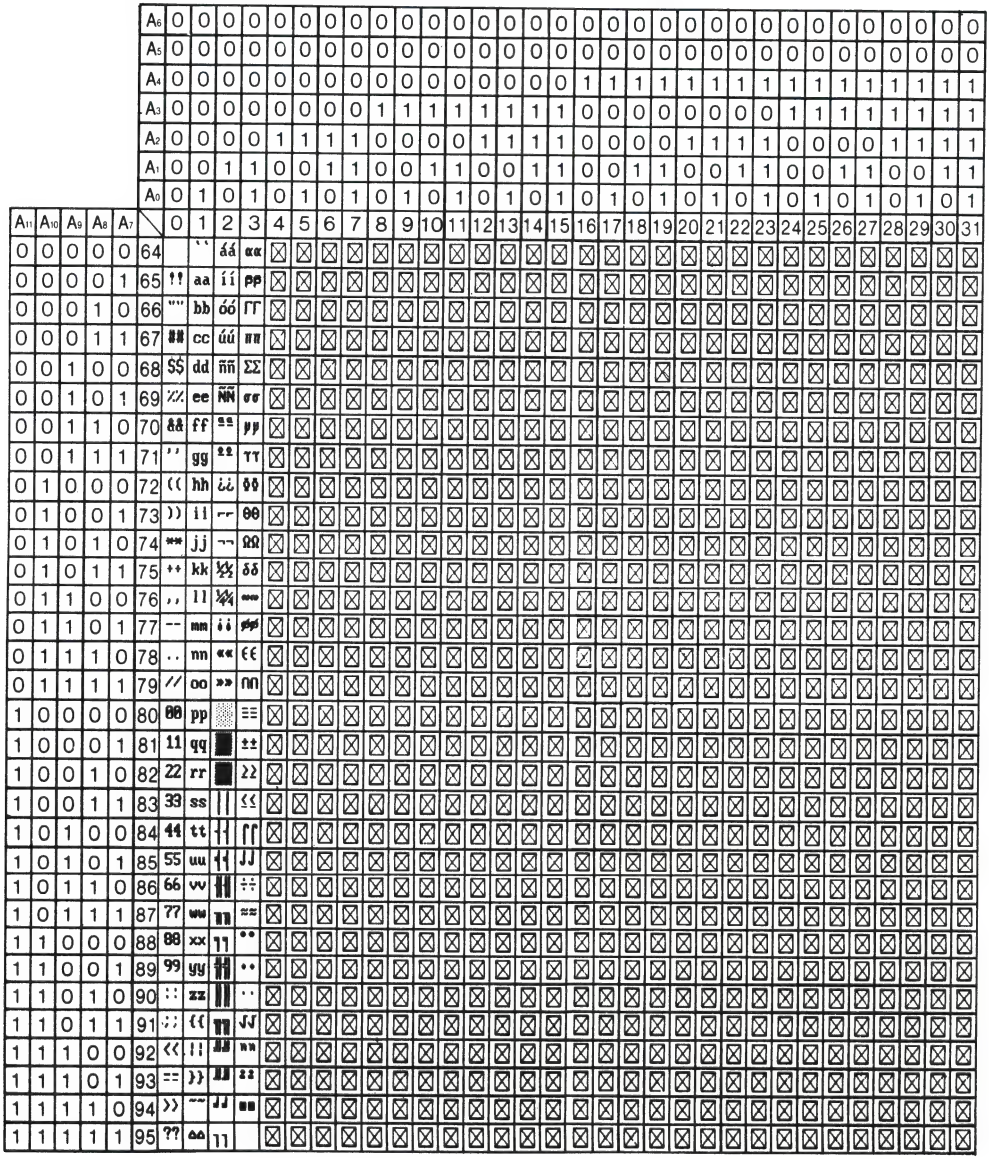
Character Allocation Table: 31A-3



Character Allocation Table: 31A-4

						96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
					A_6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					A_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					A_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					A_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A_{11}	A_{10}	A_9	A_8	A_7		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
0	0	0	0	0	32	잃	잠	잡	잣	잤	장	잦	재	잭	잰	잴	잼	잽	잿	쟀	쟁	쟈	쟉	쟌	쟙	잘	잠	장	재	잰	잴	저	적	전	절	젊	☒
0	0	0	0	1	33	춰	췄	췌	취	칙	취	췰	췸	췹	췻	츄	츈	츌	츔	츠	측	츤	츨	츰	츱	츳	층	치	칙	친	칟	칠	칡	침	칩	칫	☒
0	0	0	1	0	34	쭌	쭐	쭘	쭙	쭝	쭤	쭸	쭹	쮜	쮸	쯔	쯤	쯧	쯩	찌	찍	찐	찔	찜	찝	찡	찢	찧	차	착	찬	찮	찰	참	찹	찻	☒
0	0	0	1	1	35	축	춘	출	춤	춥	춧	충	춰	췄	췌	췐	취	췬	췰	췸	췹	췻	췽	츄	츈	출	춤	충	츠	측	츤	츨	츰	츱	츳	층	☒
0	0	1	0	0	36	콧	콩	콰	콱	콴	콸	쾀	쾅	쾌	쾡	쾨	쾰	쿄	쿠	쿡	쿤	쿨	쿰	쿱	쿳	쿵	쿼	퀀	퀄	퀑	퀘	퀭	퀴	퀵	퀸	퀼	☒
0	0	1	0	1	37	텬	텼	톄	톈	토	톡	톤	톨	톰	톱	톳	통	톺	톼	퇀	퇘	퇴	퇸	툇	툉	툐	투	툭	툰	툴	툼	툽	툿	퉁	퉈	퉴	☒
0	0	1	1	0	38	펩	펫	펬	펭	뎨	폑	펜	폘	폠	폡	폣	평	퍼	펀	펄	펌	펩	펫	펭	폐	폘	폠	폣	포	폭	폰	폴	폼	폽	폿	퐁	☒
0	0	1	1	1	39	행	햐	향	허	헉	헌	헐	헒	험	헙	헛	헝	헤	헥	헨	헬	헴	헵	헷	헹	혀	혁	현	혈	혐	협	혓	혔	형	혜	혠	☒
0	1	0	0	0	40	훈	훌	훔	훗	흉	흐	흑	흔	흠	흡	흣	흥	흩	흰	흴	희	흰	힐	힘	힙	힝	히	힉	힌	힐	힘	힙	힝	핫	항	☒
0	1	0	0	1	41	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	댸	쌰	쎄	쓔	쟀	킾	☒
0	1	0	1	0	42	間	걸	喝	曷	渴	碣	竭	葛	褐	蝎	鞨	勘	坎	堪	嵌	感	憾	戡	敢	柑	橄	減	甘	疳	監	瞰	紺	邯	鑑	鑒	龕	☒
0	1	0	1	1	43	據	擧	渠	炬	祛	距	踞	車	遽	鉅	鋸	乾	件	健	巾	建	愆	楗	腱	虔	蹇	鍵	騫	乞	傑	杰	桀	儉	劍	劒	檢	☒
0	1	1	0	0	44	瓚	瓊	痙	硬	磬	竟	競	絅	經	耕	耿	脛	莖	警	輕	逕	鏡	頃	頸	驚	鯨	係	啓	堺	契	季	屆	悸	戒	桂	械	☒
0	1	1	0	1	45	昆	梱	棍	滾	琨	袞	鯤	汨	滑	骨	供	公	共	功	孔	工	恐	恭	拱	控	攻	珙	空	蚣	貢	鞏	串	寡	戈	果	瓜	☒
0	1	1	1	0	46	僑	咬	喬	嬌	嶠	巧	攪	敎	校	橋	狡	皎	矯	絞	翹	膠	蕎	蛟	較	轎	郊	餃	驕	丘	久	九	仇	俱	具	勾	☒
0	1	1	1	1	47	宮	弓	穹	窮	芎	躬	倦	券	勸	卷	圈	拳	捲	權	淃	眷	厥	獗	蕨	蹶	闕	机	櫃	潰	詭	軌	饋	句	晷	龜	貴	☒
1	0	0	0	0	48	及	急	扱	汲	級	給	亘	兢	矜	肯	企	伎	其	冀	嗜	器	圻	基	埼	夔	奇	妓	寄	岐	崎	己	幾	忌	技	旗	既	☒
1	0	0	0	1	49	邁	那	樂	洛	烙	珞	落	諾	酪	駱	亂	卵	暖	欄	煖	爛	蘭	難	鸞	捏	捺	南	嵐	枏	楠	湳	濫	男	藍	襤	拉	☒
1	0	0	1	0	50	腦	賂	雷	尿	壘	屢	樓	淚	漏	累	縷	陋	嫩	訥	杻	紐	勒	肋	凜	凌	稜	綾	能	菱	陵	尼	泥	匿	溺	多	茶	☒
1	0	0	1	1	51	岱	帶	待	戴	擡	玳	臺	袋	貸	隊	黛	宅	德	悳	倒	刀	到	圖	堵	塗	導	屠	島	嶋	度	徒	悼	挑	掉	搗	桃	☒
1	0	1	0	0	52	斗	杜	枓	痘	竇	荳	讀	豆	逗	頭	屯	臀	芚	遁	遯	鈍	得	嶝	橙	燈	登	等	藤	謄	鄧	騰	喇	懶	拏	癩	羅	☒
1	0	1	0	1	53	輛	量	侶	儷	勵	呂	廬	慮	戾	旅	櫚	濾	礪	藜	蠣	閭	驢	驪	麗	黎	力	曆	歷	瀝	碌	礫	轢	靈	憐	戀	攣	漣	☒
1	0	1	1	0	54	線	彙	錄	鹿	麓	論	壟	弄	朧	瓏	籠	聾	儡	瀨	牢	磊	賂	賚	賴	雷	了	僚	寮	廖	料	燎	瞭	聊	蓼	遼	☒
1	0	1	1	1	55	梨	狸	理	瓈	異	痢	罹	羸	莉	裏	裡	里	釐	離	鯉	吝	潾	燐	璘	藺	躪	隣	鱗	林	淋	琳	臨	霖	砬	☒
1	1	0	0	0	56	煤	黴	買	賣	邁	魅	脈	貊	陌	驀	麥	孟	氓	猛	盲	盟	萌	冪	覓	免	冕	勉	棉	沔	眄	眠	綿	緬	面	麵	滅	☒
1	1	0	0	1	57	苗	錨	務	巫	憮	憮	戊	拇	撫	无	楙	武	毋	無	珷	畝	繆	舞	茂	蕪	誣	貿	霧	鵡	墨	默	們	刎	吻	問	文	☒
1	1	0	1	0	58	殿	伴	半	反	叛	拌	攀	蟠	班	槃	泮	潘	班	畔	瘢	盤	盼	磐	磻	礬	絆	般	蟠	返	頒	飯	勃	拔	撥	渤	潑	☒
1	1	0	1	1	59	樊	煩	燔	番	磻	繁	蕃	藩	飜	伐	筏	罰	閥	凡	帆	梵	氾	汎	泛	犯	範	范	法	琺	僻	劈	壁	擘	檗	癖	☒
1	1	1	0	0	60	飜	飜	本	奔	犇	傰	奉	封	峯	峰	捧	棒	烽	熢	琫	縫	蓬	蜂	逢	鋒	鳳	不	付	俯	傅	剖	副	否	吩	咐	埠	夫	婦	☒
1	1	1	0	1	61	丕	備	匕	匪	卑	妃	婢	庇	悲	憊	扉	批	斐	枇	榧	比	毖	毗	毘	沸	泌	琵	痺	砒	碑	秕	秘	粑	緋	翡	肥	☒
1	1	1	1	0	62	澁	瀉	獅	砂	社	祀	祠	私	篩	紗	絲	辭	舍	莎	裟	蛇	裟	詐	詞	謝	賜	赦	辭	邪	飼	駟	麝	削	數	朔	索	☒
1	1	1	1	1	63	蔴	塞	穡	索	色	牲	生	甥	省	笙	墅	壻	嶼	序	庶	徐	恕	抒	捿	敍	暑	曙	書	栖	棲	犀	瑞	筮	絮	緖	署	☒

Character Allocation Table: 32A-1



Character Allocation Table: 32A-2

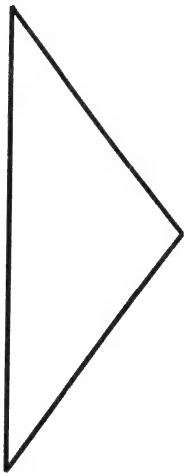
					A_6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					A_5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					A_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					A_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					A_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A_{11}	A_{10}	A_9	A_8	A_7		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
0	0	0	0	0	64	☒	胥	舒	薯	西	誓	逝	鋤	黍	鼠	夕	奭	席	惜	昔	晳	析	汐	淅	潟	石	碩	蓆	釋	錫	仙	僊	先	善	嬋	宣	扇
0	0	0	0	1	65	☒	聖	聲	腥	誠	醒	世	勢	歲	洗	稅	笹	細	說	貰	召	嘯	塑	宵	小	少	巢	所	掃	搔	昭	梳	沼	消	溯	瀟	炤
0	0	0	1	0	66	☒	戍	手	授	搜	收	數	樹	殊	水	洙	漱	燧	狩	獸	琇	璲	瘦	睡	秀	穗	竪	粹	綏	綬	繡	羞	脩	茱	蒐	蓚	藪
0	0	0	1	1	67	☒	嵩	瑟	膝	蝨	濕	拾	習	褶	襲	丞	乘	僧	勝	升	承	昇	繩	蠅	陞	侍	匙	嘶	始	媤	尸	屎	屍	市	弑	恃	施
0	0	1	0	0	68	☒	沈	深	瀋	甚	芯	諶	什	十	拾	雙	氏	亞	俄	兒	啞	娥	峨	我	牙	芽	莪	蛾	衙	訝	阿	雅	餓	鴉	鵝	堊	岳
0	0	1	0	1	69	☒	櫻	罌	鶯	鸚	也	倻	冶	夜	惹	揶	椰	爺	耶	若	野	弱	掠	略	約	若	葯	蒻	藥	躍	亮	佯	兩	凉	壤	孃	恙
0	0	1	1	0	70	☒	旅	歟	汝	濾	璵	礖	礪	與	艅	茹	輿	轝	閭	餘	驪	麗	黎	亦	力	域	役	易	曆	歷	疫	繹	譯	轢	逆	驛	嚥
0	0	1	1	1	71	☒	簾	閻	髥	鹽	曄	獵	燁	葉	令	囹	塋	寧	嶺	嶸	影	怜	映	暎	楹	榮	永	泳	渶	潁	濚	瀛	瀯	煐	營	獰	玲
0	1	0	0	0	72	☒	烏	熬	獒	筽	蜈	誤	鰲	鼇	屋	沃	獄	玉	鈺	溫	瑥	瘟	穩	縕	蘊	兀	壅	擁	瓮	甕	癰	翁	邕	雍	饔	渦	瓦
0	1	0	0	1	73	☒	窈	窯	繇	繞	耀	腰	蓼	蟯	要	謠	遙	遼	邀	饒	慾	欲	浴	縟	褥	辱	俑	傭	冗	勇	埇	墉	容	庸	慂	榕	涌
0	1	0	1	0	74	☒	運	隕	雲	韻	蔚	鬱	亐	熊	雄	元	原	員	圓	園	垣	媛	嫄	寃	怨	愿	援	沅	洹	湲	源	爰	猿	瑗	苑	袁	轅
0	1	0	1	1	75	☒	濡	猶	猷	琉	瑜	由	留	癒	硫	紐	維	臾	萸	裕	誘	諛	諭	踰	蹂	遊	逾	遺	酉	釉	鍮	類	六	堉	戮	毓	肉
0	1	1	0	0	76	☒	議	醫	二	以	伊	利	吏	夷	姨	履	已	弛	彛	怡	易	李	梨	泥	爾	珥	理	異	痍	痢	移	罹	而	耳	肄	苡	荑
0	1	1	0	1	77	☒	立	笠	粒	仍	剩	孕	芿	仔	刺	咨	姉	姿	子	字	孜	恣	慈	滋	炙	煮	玆	瓷	疵	磁	紫	者	自	茨	蔗	藉	諮
0	1	1	1	0	78	☒	障	再	哉	在	宰	才	材	栽	梓	渽	滓	災	縡	裁	財	載	齋	齎	爭	箏	諍	錚	佇	低	儲	咀	姐	底	抵	杵	楮
0	1	1	1	1	79	☒	煎	琠	田	甸	畑	癲	筌	箋	箭	篆	纏	詮	輾	轉	鈿	銓	錢	鐫	電	顚	顫	餞	切	截	折	浙	癤	竊	節	絶	占
1	0	0	0	0	80	☒	靜	頂	鼎	制	劑	啼	堤	帝	弟	悌	提	梯	濟	祭	第	臍	薺	製	諸	蹄	醍	除	際	霽	題	齊	俎	兆	凋	助	嘲
1	0	0	0	1	81	☒	踪	踵	鍾	鐘	佐	坐	左	座	挫	罪	主	住	侏	做	姝	胄	呪	周	嗾	奏	宙	州	廚	晝	朱	柱	株	注	洲	湊	澍
1	0	0	1	0	82	☒	咫	地	址	志	持	指	摯	支	旨	智	枝	枳	止	池	沚	漬	知	砥	祉	祗	紙	肢	脂	至	芝	芷	蜘	誌	識	贄	趾
1	0	0	1	1	83	☒	鏶	集	徵	懲	澄	且	侘	借	叉	嗟	嵯	差	次	此	磋	箚	茶	蹉	車	遮	捉	搾	着	窄	錯	鑿	齪	撰	澯	燦	璨
1	0	1	0	0	84	☒	責	凄	妻	悽	處	倜	刺	剔	尺	慽	戚	拓	擲	斥	滌	瘠	脊	蹠	陟	隻	仟	千	喘	天	川	擅	泉	淺	玔	穿	舛
1	0	1	0	1	85	☒	椒	楚	樵	炒	焦	硝	礁	礎	秒	稍	肖	艸	苕	草	蕉	貂	超	酢	醋	醮	促	囑	燭	矗	蜀	觸	寸	忖	村	邨	叢
1	0	1	1	0	86	☒	贅	取	吹	嘴	娶	就	炊	翠	聚	脆	臭	趣	醉	驟	鷲	側	仄	厠	惻	測	層	侈	値	嗤	峙	幟	恥	梔	治	淄	熾
1	0	1	1	1	87	☒	鐸	呑	嘆	坦	彈	憚	歎	灘	炭	綻	誕	奪	脫	探	眈	耽	貪	塔	搭	榻	宕	帑	湯	糖	蕩	兌	台	太	怠	態	殆
1	1	0	0	0	88	☒	阪	八	叭	捌	佩	唄	悖	敗	沛	浿	牌	狽	稗	覇	貝	彭	澎	烹	膨	愎	便	偏	扁	片	篇	編	翩	遍	鞭	騙	貶
1	1	0	0	1	89	☒	品	稟	楓	諷	豊	風	馮	彼	披	疲	皮	被	避	陂	匹	弼	必	泌	珌	畢	疋	筆	苾	馝	乏	逼	下	何	厦	夏	廈
1	1	0	1	0	90	☒	行	降	項	亥	偕	咳	垓	奚	孩	害	懈	楷	海	瀣	蟹	解	該	諧	邂	駭	骸	劾	核	倖	幸	杏	荇	行	享	向	嚮
1	1	0	1	1	91	☒	形	泂	滎	瀅	灐	炯	熒	珩	瑩	荊	螢	衡	逈	邢	鎣	馨	兮	彗	惠	慧	暳	蕙	蹊	醯	鞋	乎	互	呼	壕	壺	好
1	1	1	0	0	92	☒	禍	禾	花	華	話	譁	貨	靴	廓	擴	攫	確	碻	穫	丸	喚	奐	宦	幻	患	換	歡	晥	桓	渙	煥	環	紈	還	驩	鰥
1	1	1	0	1	93	☒	爻	肴	酵	驍	侯	候	厚	后	吼	喉	嗅	帿	後	朽	煦	珝	逅	勛	勳	塤	壎	焄	熏	燻	薰	訓	暈	薨	喧	暄	煊
1	1	1	1	0	94	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒
1	1	1	1	1	95	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒

Character Allocation Table: 32A-3

					A_6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					A_4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
					A_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
					A_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
					A_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
A_{11}	A_{10}	A_9	A_8	A_7		64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
0	0	0	0	0	64	勘	旋	渦	煽	琁	瑄	璇	璋	癬	禪	線	繕	羨	腺	膳	船	蘚	蟬	詵	跣	選	銑	鐥	饌	鮮	卣	屑	楔	泄	洩	渫	舌
0	0	0	0	1	65	焼	甦	疏	疎	痩	笑	篠	簫	素	紹	蔬	蕭	蘇	訴	逍	遡	邵	銷	韶	騒	俗	屬	束	涑	粟	續	謖	贖	速	孫	巽	損
0	0	0	1	0	66	袖	誰	警	輸	遂	邃	酬	銖	銹	隋	隧	隨	雖	需	須	首	髄	鬚	叔	塾	夙	孰	宿	淑	潤	熟	琡	璹	粛	蒋	巡	徇
0	0	0	1	1	67	是	時	梔	柴	猜	矢	示	翔	蒔	蒼	視	試	詩	諡	豕	豺	埴	寔	式	息	拭	植	殖	湜	熄	篒	蝕	識	軾	食	飾	伸
0	0	1	0	0	68	嶄	幌	惹	愕	握	樂	渥	鄂	鍔	顎	鰐	齷	安	岸	按	晏	案	眼	雁	鞍	顔	鮟	鋲	謁	軋	閼	唵	岩	巌	庵	暗	癌
0	0	1	0	1	69	揚	擾	敷	暘	梁	楊	様	洋	濆	煬	痒	瘍	禳	穣	糧	羊	良	襄	諒	譲	醸	陽	量	養	圖	御	於	漁	瘀	禦	語	馭
0	0	1	1	0	70	塙	妍	娟	寞	年	延	憐	戀	捐	挺	撚	椽	沇	沿	涎	涓	淵	演	漣	烟	然	煙	煉	燃	燕	璉	研	硯	秊	筵	緣	練
0	0	1	1	1	71	瑛	瑩	瓔	盈	穎	纓	羚	聆	英	詠	迎	鈴	鍈	霙	霊	靈	領	乂	倪	例	刈	叡	曳	汭	濊	猊	嘗	穢	芮	蘂	褻	禮
0	1	0	0	0	72	冨	釐	臥	蛙	蝸	詭	嫄	宛	椀	椀	浣	玩	琉	琓	碗	緩	翫	晥	腕	莞	豌	阮	頑	曰	往	旺	柱	汪	王	倭	娃
0	1	0	0	1	73	溳	溶	熔	瑢	用	甬	畿	茸	蓉	踊	鎔	鏞	龍	于	佑	偶	優	又	友	右	宇	寓	尤	愚	憂	旴	牛	玗	瑀	盂	祐	禑
0	1	0	1	0	74	遠	阮	院	願	鴛	月	越	鉞	位	偉	僞	危	圍	委	威	尉	慰	暐	渭	爲	瑋	緯	胃	萎	葦	蔚	蝟	衛	褘	謂	違	韋
0	1	0	1	1	75	育	陸	倫	允	淪	尹	紊	淪	潤	玩	胤	贇	輪	鈗	閏	律	慄	栗	率	聿	戎	瀜	絨	融	隆	垠	恩	慇	殷	誾	銀	隱
0	1	1	0	0	76	裏	裡	貽	貳	遝	里	離	飴	餌	匿	溺	瀷	益	翊	翌	翼	謚	人	仁	刃	印	吝	咽	因	姻	寅	引	忍	湮	燐	璘	絪
0	1	1	0	1	77	資	雌	作	勺	嚼	斫	昨	灼	炸	爵	綽	芍	酌	雀	鵲	孱	棧	殘	潺	盞	岑	暫	潛	箴	簪	蠶	雜	丈	仗	匠	場	墻
0	1	1	1	0	78	樗	沮	渚	狙	猪	疽	箸	紵	苧	菹	著	藷	詛	貯	躇	這	邸	雎	齟	勣	吊	嫡	寂	摘	敵	滴	狄	炙	的	積	笛	籍
0	1	1	1	1	79	岾	店	漸	点	粘	霑	鮎	點	接	摺	蝶	丁	井	亭	停	偵	呈	廷	悌	庭	廷	征	情	挺	政	整	旌	晶	晸	柾	楨
1	0	0	0	0	80	弔	彫	措	操	早	晁	曺	曹	朝	條	棗	槽	漕	潮	照	燥	爪	璪	眺	祖	祚	租	稠	窕	粗	糟	組	繰	壔	藻	蚤	詔
1	0	0	0	1	81	烓	珠	噣	簇	紂	紬	綢	舟	蛛	註	誅	走	躊	輳	週	酎	酒	鋳	駐	竹	粥	俊	儁	准	埈	寯	峻	晙	樽	浚	準	濬
1	0	0	1	0	82	遷	直	稙	稷	織	職	唇	嚞	麈	振	搢	晉	晋	桭	榛	殄	津	溱	珍	瑨	璡	畛	疹	盡	眞	瞋	秦	縉	縝	臻	蔯	袗
1	0	0	1	1	83	瓚	顓	蔗	篡	粲	纘	讚	贊	鑽	餐	饌	刹	察	擦	札	紮	僭	參	塹	慘	慙	懺	斬	站	讒	讖	倉	倡	創	唱	娼	廠
1	0	1	0	0	84	薦	賤	踐	遷	釧	闡	阡	韆	凸	哲	喆	徹	撤	澈	綴	輒	轍	鐵	僉	尖	沾	添	甜	瞻	簽	籤	詹	諜	堞	妾	帖	捷
1	0	1	0	1	85	塚	寵	悤	憁	摠	總	聰	蔥	銃	撮	催	崔	最	墜	抽	推	椎	楸	樞	湫	鰍	秋	芻	萩	諏	趨	追	鄒	酋	醜	錐	錘
1	0	1	1	0	86	痔	痴	癡	稚	穉	緇	緻	置	致	蚩	輜	雉	馳	齒	則	軔	飭	親	七	柒	漆	侵	寢	杭	沈	浸	琛	砧	針	鍼	蟄	秤
1	0	1	1	1	87	汰	泰	笞	胎	苔	跆	邰	颱	宅	擇	澤	撑	攄	兎	吐	土	討	慟	桶	洞	痛	筒	統	通	堆	槌	腿	褪	退	頹	偸	套
1	1	0	0	0	88	坪	平	枰	萍	評	吠	嬖	幣	廢	弊	斃	肺	蔽	閉	陛	佈	包	匍	匏	咆	哺	圃	布	怖	抛	抱	捕	暴	泡	浦	疱	砲
1	1	0	0	1	89	昰	河	瑕	荷	蝦	賀	遐	霞	鰕	壑	學	虐	謔	鶴	寒	恨	悍	旱	汗	漢	澣	瀚	罕	翰	閑	閒	限	韓	割	轄	函	含
1	1	0	1	0	90	珦	鄕	響	餉	饗	香	噓	墟	虛	許	憲	櫶	獻	軒	歇	險	驗	奕	爀	赫	革	俔	峴	弦	懸	晛	泫	炫	玄	玹	現	眩
1	1	0	1	1	91	蚶	弧	戶	扈	昊	晧	毫	濠	浩	溷	滈	皓	祜	瀇	濩	狐	琥	瑚	瓠	皓	祜	糊	縞	胡	芦	葫	蒿	虎	號	蝴	護	豪
1	1	1	0	0	92	活	滑	猾	豁	闊	凰	幌	徨	恍	惶	愰	滉	漾	煌	璜	皇	篁	簧	荒	蝗	遑	隍	黄	匯	回	廻
1	1	1	0	1	93	萱	卉	喙	毁	彙	徽	揮	暉	煇	諱	輝	麾	休	携	烋	畦	虧	恤	譎	鷸	兇	凶	匈	洶	胸	黑	昕	欣	炘	痕	吃	屹
1	1	1	1	0	94	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒
1	1	1	1	1	95	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒

Character Allocation Table: 32A-4

					A6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
					A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A11	A10	A9	A8	A7		96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
0	0	0	0	0	64	薛	褻	設	說	雪	齧	剡	暹	殲	纖	蟾	贍	閃	陝	攝	涉	燮	葉	城	姓	宬	性	惺	成	星	晟	猩	珹	盛	省	筬	⊠
0	0	0	0	1	65	蓀	遜	飡	率	宋	悚	松	淞	訟	誦	送	頌	刷	殺	灑	碎	鎖	衰	釗	修	受	嗽	囚	垂	壽	嫂	守	岫	峀	帥	愁	⊠
0	0	0	1	0	66	循	恂	旬	栒	楯	橓	殉	洵	淳	珣	盾	瞬	筍	純	脣	舜	荀	蓴	蕣	詢	諄	醇	錞	順	馴	戌	術	述	鉥	崇	崧	⊠
0	0	0	1	1	67	侁	信	呻	娠	宸	愼	新	晨	燼	申	神	紳	腎	臣	莘	薪	藎	蜃	訊	身	辛	辰	迅	失	室	實	悉	審	尋	心	沁	⊠
0	0	1	0	0	68	菴	闇	壓	押	狎	鴨	仰	央	怏	昻	殃	秧	鴦	厓	哀	埃	崖	愛	曖	涯	碍	艾	隘	靄	厄	扼	掖	液	縊	腋	額	⊠
0	0	1	0	1	69	魚	齬	億	憶	抑	檍	臆	偃	堰	彦	焉	言	諺	孼	蘖	俺	儼	嚴	奄	掩	淹	嶪	業	円	予	余	勵	呂	女	如	廬	⊠
0	0	1	1	0	70	縯	聯	衍	軟	輦	蓮	連	鉛	鍊	鳶	列	劣	咽	悅	涅	烈	熱	裂	說	閱	厭	廉	念	捻	染	殮	炎	焰	琰	艶	苒	⊠
0	0	1	1	1	71	裔	詣	譽	豫	醴	銳	隸	霓	預	五	伍	俉	傲	午	吾	吳	嗚	塢	墺	奧	娛	寤	悟	惡	懊	敖	旿	晤	梧	汚	澳	⊠
0	1	0	0	0	72	歪	矮	外	嵬	巍	猥	畏	了	僚	僥	凹	堯	夭	妖	姚	寥	寮	尿	嶢	拗	搖	撓	擾	料	曜	樂	橈	燎	燿	瑤	療	⊠
0	1	0	0	1	73	禹	紆	羽	芋	藕	虞	迂	遇	郵	釪	隅	雨	雩	勖	彧	旭	昱	栯	煜	稶	郁	頊	云	暈	橒	殞	澐	熉	耘	芸	蕓	⊠
0	1	0	1	0	74	魏	乳	侑	儒	兪	劉	唯	喩	孺	宥	幼	幽	庾	悠	惟	愈	愉	揄	攸	有	杻	柔	柚	柳	楡	楢	油	洧	流	游	溜	⊠
0	1	0	1	1	75	乙	吟	淫	蔭	陰	音	飮	揖	泣	邑	凝	應	膺	鷹	依	倚	儀	宜	意	懿	擬	椅	毅	疑	矣	義	艤	薏	蟻	衣	誼	⊠
0	1	1	0	0	76	茵	藺	蚓	認	隣	靭	靷	鱗	麟	一	佚	佾	壹	日	溢	逸	鎰	馹	任	壬	妊	姙	恁	林	淋	稔	臨	荏	賃	入	卄	⊠
0	1	1	0	1	77	壯	奬	將	帳	庄	張	掌	暲	杖	樟	檣	欌	漿	牆	狀	獐	璋	章	粧	腸	臟	臧	莊	葬	蔣	薔	藏	裝	贓	醬	長	⊠
0	1	1	1	0	78	績	翟	荻	謫	賊	赤	跡	蹟	迪	迹	適	鏑	佃	佺	傳	全	典	前	剪	塡	塼	奠	專	展	廛	悛	戰	栓	殿	氈	澱	⊠
0	1	1	1	1	79	檉	正	汀	淀	淨	渟	湞	瀞	炡	玎	珽	町	睛	碇	禎	程	穽	精	綎	艇	訂	諪	貞	鄭	酊	釘	鉦	鋌	錠	霆	靖	⊠
1	0	0	0	0	80	調	趙	躁	造	遭	釣	阻	雕	鳥	族	簇	足	鏃	存	尊	卒	拙	猝	倧	宗	從	悰	慫	棕	淙	琮	種	終	綜	縱	腫	⊠
1	0	0	0	1	81	焌	畯	竣	蠢	逡	遵	雋	駿	茁	中	仲	衆	重	卽	櫛	楫	汁	葺	增	憎	曾	拯	烝	甑	症	繒	蒸	證	贈	之	只	⊠
1	0	0	1	0	82	診	賑	軫	辰	進	鎭	陣	陳	震	侄	叱	姪	嫉	帙	桎	瓆	疾	秩	窒	膣	蛭	質	跌	迭	斟	朕	什	執	潗	緝	輯	⊠
1	0	0	1	1	83	彰	愴	敞	昌	昶	暢	槍	滄	漲	猖	瘡	窓	脹	艙	菖	蒼	債	埰	寀	寨	彩	採	砦	綵	菜	蔡	采	釵	冊	柵	策	⊠
1	0	1	0	0	84	牒	疊	睫	諜	貼	輒	廳	晴	淸	聽	菁	請	靑	鯖	切	剃	替	涕	滯	締	諦	逮	遞	體	初	剿	哨	憔	抄	招	梢	⊠
1	0	1	0	1	85	鎚	雛	騶	鰍	丑	畜	祝	竺	筑	築	縮	蓄	蹙	蹴	軸	逐	春	椿	瑃	出	朮	黜	充	忠	沖	蟲	衝	衷	悴	膵	萃	⊠
1	0	1	1	0	86	稱	快	他	咤	唾	墮	妥	惰	打	拖	朶	楕	舵	陀	馱	駝	倬	卓	啄	坼	度	托	拓	擢	晫	柝	濁	濯	琢	琸	託	⊠
1	0	1	1	1	87	妬	投	透	鬪	慝	特	闖	坡	婆	巴	把	播	擺	杷	波	派	爬	琶	破	罷	芭	跛	頗	判	坂	板	版	瓣	販	辦	鈑	⊠
1	1	0	0	0	88	胞	脯	苞	葡	蒲	袍	褒	逋	鋪	飽	鮑	幅	暴	曝	瀑	爆	輻	俵	剽	彪	慓	杓	標	漂	瓢	票	表	豹	飇	飄	驃	⊠
1	1	0	0	1	89	咸	啣	喊	檻	涵	緘	艦	銜	陷	鹹	合	哈	盒	蛤	閤	闔	陜	亢	伉	姮	嫦	巷	恒	抗	杭	桁	沆	港	缸	肛	航	⊠
1	1	0	1	0	90	睍	絃	絢	縣	舷	衒	見	賢	鉉	顯	孑	穴	血	頁	嫌	俠	協	夾	峽	挾	浹	狹	脅	脇	莢	鋏	頰	亨	兄	刑	型	⊠
1	1	0	1	1	91	鎬	頀	顥	惑	或	酷	婚	昏	混	渾	琿	魂	忽	惚	笏	哄	弘	汞	泓	洪	烘	紅	虹	訌	鴻	化	和	嬅	樺	火	畵	⊠
1	1	1	0	0	92	徊	恢	悔	懷	晦	會	檜	淮	澮	灰	獪	繪	膾	茴	蛔	誨	賄	劃	獲	宖	橫	鐄	哮	嚆	孝	效	斅	曉	梟	涍	淆	⊠
1	1	1	0	1	93	紇	訖	欠	欽	歆	吸	恰	洽	翕	興	僖	凞	喜	噫	囍	姬	嬉	希	憙	憘	戱	晞	曦	熙	熹	熺	犧	禧	稀	羲	詰	⊠
1	1	1	1	0	94	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠
1	1	1	1	1	95	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠



Q A MANUAL

CONTENTS

1. INTRODUCTION

In recent years, advances in intergrated circuit have been rapid with increasing density and speed accompanied by decreasing cost. To meet these advances, there are three basic ingredients in the manufacture of reliable integrated circuits.

First, The device must be designed with the user's applications and reliability reguirements in mind. Secondly, The device must be manufactured with the optimum technology for the application. Thirdly, Controls must be established to assure maintenance of the quality/reliability levels. GoldStar Semiconductor has a Quality Assurance System and conducts extensive reliability testing to supply it's customer's needs.

This report presents Quality Assurance System and Reliability test results of GoldStar Semiconductor Company Products.

2. QUALITY ASSURANCE SYSTEM

To ensure that customers are satisfied with the products that are supplied, quality assurance programs are used at both the design and manufacturing phases, focusing on the following points:

(1) In the development stage, reliability is designed into prdoucts. A through evaluation of reliability is performed to ascertain whether the design will lead to the desired quality and reliability.

(2) Efforts are made at the manufacturing stage of quality control to assure that quality and reliability are built into products. Intermediate, final, and quality assurance inspection are used to verify that the desired quality and reliability have been achieved.

(3) Information with regard to quality is fed back in a timely manner so that the required corrective action can be taken by quality assurance personal.

2.1 Quality Assurance at the Development Stage

It is not an exaggeration to say that the fundamental quality and reliability of a discrete semiconductor device or an intergrated circuit is determined at the design stage. Thus, to eliminate design problems and provide design improvements while attaining the desired quality and reliability, design reviews are performed on prototypes assure product quality. Particularly in the case of intergrated circuits, breadboard models of the circuit using standard components can be an effective means of evaluating the required characteristic and quality. In addition CAD technology may be used to aid in the design of circuits and devices based on design standards.

Between the development stage, and mass production, there are two steps of prototype and preproduction (trial mass production).

At the prototype development stage, new theories, technologies and concepts are used by the development department to design and produce a new product. To determine whether the desired goals for characterstics, ratings, and reliability have been met, primary type test is performed at this stage. Based on these results, through investigations are made by both the engineering and quality assurance departments. Should product deficiencies arise, inspections and failure analysis are performed to enable improvements of the development prototype.

At the pre-production stage, the production department produces sufficient products having quality equal to or superior to the prototype. At this stage, secondary type test is used to verify quality. The required product specifications, operation instructions, drawings, etc, are produce at this stage in addition to the required manufacturing facilities.

2.2. Quality Assurance at the Mass Production Stage

At the mass production stage, the production department takes over production of product based on production planning. To maintain equal or better quality than that obtained in previous stages, careful control of materials purchasing, production processing, environment and facilities is performed. In addition, in process inspections and final inspections provide the required information with regard to partiality completed and completed devices to assure overall quality.

2.2.1. Control of Materials Purchasing

While the responsibility for quality of individual materials purchased from vendors based on materials and specifications is that of the vendor, the corporation provides data from incoming inspection of sampled products as a means of monitoring quality and assuring materials quality. Selection of vendors is made adopter an investigation of quality control and assurance system, management, facilities and production capacity of the vendor, placing heavy emphasis on quality. Next, a meeting is held with the vendor concerning the purchase specification, and prototypes or sample evaluations are used to verify quality at the beginning or a purchase cycle or after a change in manufacturing method or specifications.

When a material is put into warehouse incoming inspection section receives COC (Certificate Of Compliance) and COA (Certificate Of Analysis) from vendor and evaluates the material according to above two documents authorized by issued material and incoming inspection specification.

2.2.2 Control of the Manufacturing Process

To prototype products of high quality in an economic manner, quality must be built-in at the manutacturing stage. To do this, work is carried out in accordance with specification controlled and control charts are used to control those aspects of manufacturing that could affect quality.
For example such information as the purity of DI water and chemicals, gas flow, atomosphere, equipment calibration, particles emitted equipment is recorded.

Inprocess inspections and final inspection are performed to evaluate product quality including outward appearance, dimensions, structure, aswell as mechanical and electrical characteristics. The data obtained by such inspections is fed back to earlier processes to maintain and improve product quality as well as reduce variations in these areas. When is out of quality control inspection specifications, that run is scraped to maintain quality specification. Wafer processing and assembly inspections is performed, and each contributing to the concept of building in quality at the manufacturing stage by providing self checks and the inspections performed by the quality control department. A final inspection of all products is performed to verify electrical characteristics as well as outward appearance of products. In addition, to improve product quality uniformity, debugging is used as a means of eliminating products which to not meet quality specifications. Again, data from these inspections are useful in quality control.

Products which have passed final inspectin are then subjected to quality assurance inspections. This is a form of overall inspection from the standpoint of the end user and is used to the end user and is used to accept or reject products on a lot basis, including tests of outward appearance, electrical characteristics, thermal and mechanical environment, and endurance. As an additional control test, samples are made periodically for evaluation of reliability.
These tests include those of electrical characterics, thermal and mechanical environment, and endurance for long periods of operation.

The information on quality obtained by such quality assurance inspectins is fed back in a timely fashion to the related department, enabling the maintenance and improvement of quality as well as providing a means of predicting product quality in the market place.

2.2.3. Environmental Control

In the semiconductor industry, the environment plays a large role in influencing product quality and reliability. Control levels for dust humidity and temperature are set and rigidly maintained.
The gases or water used in the production plant are carefully controlled to ensure high level of purity.
The items periodically checked by quality control are such as fabrication atmosphere, equipments, chemicals, air flow and the temperature, resistivity bacteria, particle, contaminations total organic carbon, silica etc. related to DI water.
The control of particle and temperature is particularly impotant in reducing manufacturing defects and improving quality and reliability. For this reason the corporation places heavy emphasis in this area, providing strict controls of working conditions and periodic checks to verify that these are being maintained.

2.2.4. Control of Production Equipment and Calibration

The semiconductor industry is an equipment intensive industry having adopted a large variety of automatic equipment and high performance facilities to provide uniform high quality.
The control of such equipment and instrumentation is extremely important in the manufacture of devices. For this reason to eliminate loss of accuracy and equipment failures, periodic preventive maintenance calibrations are performed.

Calibrations are performed to all measurement equipments and classified into self performing calibration and external official calibration performed by certified public authorities. The self performing libration is periodically performed by standard sample comparable with NBS (National Bureau of Standard) and the external official calibration is performed by inserting the standard cell into the measurement equipments to know whether the equipments are in good quality condition or not and if they aren't in good condition they need calibrating.

2.2.5. Control of Specification & Documentation

Such procedure as equipment operation, maintenance, all process procedures and all materials, and the other works related to quality is defined by specifications.
The specification documents are defined, controlled, authorized, distributed, released, and are audited by quality assurance section.

2.2.6. Training & Audit

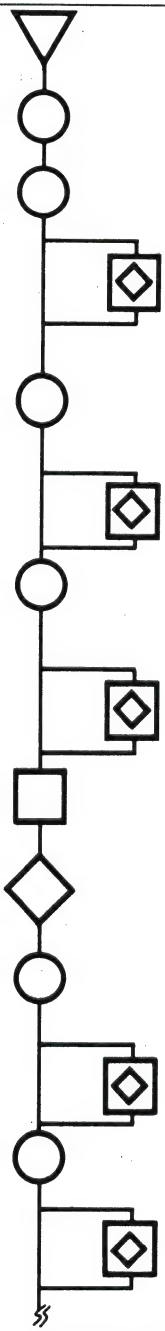
In semiconductor manufacturing one of the important factors is man power. All operators related to quality directly or indirectly are periodically trained by engineers/supervisors, and they are also trained when the processes or procedures are changed.
All records are preserved. Each process are contains only the members who are certified by training and qualification evaluation.

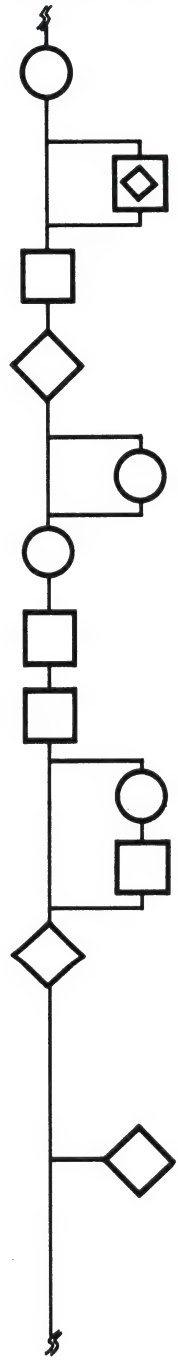
Quality assurance section periodically audit fabrication area, to know whether all specifications are kept or not. All audit records are noticed to production department a corrective action is made and fed back to each process area.

** Process Evaluation System In Wafer Fabrication **

PROCESS	EQUIPMENT EVALUATION	PROCESS EVALUATION
W/F INPUT		Resistivity, Thickness, Defects Documents, Visual inspection
CLEANING	Particle check	Thickness Visual (Particle) Inspection
OXIDATION	Particle check Temperature check C-V test	Field/Total Oxidation Thickness Visual Inspection
PHOTO- LITHOGRAPHY	Mask: Defects Patterns Particle check Aligner: Focus, Distortion Resolution Coater: Photoresist thickness exhaust	CD check Development Inspection
DIFFUSION	Temperature check C-V test Particle check	Sheet Resistivity Diffusion Depth
ION IMPLANTATION	Particle check V/I check Utility check	
SPUTTERING	Particle check Utility check C-V test	Thickness, Rs (or V/I)
ETCH	Temperature check Particle check Uniformity check	Thickness, CD Check Visual Inspection
PARAMETER TEST		Contact String, Sheet Resistance Threshold Voltage, Breakdown Voltage

STANDARD ASS'Y FLOW CHART OF GSS

FLOW CHART	PROCESS TITLE	QC POINT
	Wafer	
	Foil Mount	
	Wafer Sawing	
	Q.C Monitor * DI Water * Visual	RESISTIVITY VISIUAL
	Die Bond	
	Q.C Monitor * Visual * Die Shear	APPEARANCE STRENGTH
	Wire Bond	
	Q.C Monitor * Visual * Bond pull * Crater	APPEARANCE APPEARANCE, STRENGTH CRATER
	3rd Optical Insp.	
	Q.C 3/0 gate * Visual	APPEARANCE
	Molding	SPRIAL FLOW
	Q.C Monitor * Visual * X-Ray Monitor	APPEARANCE X-RAY INSP.
	Deflash/Trim/Form	
	Q.C Monitor * Visual/Dimension	APPEARANCE/DIMENSION

FLOW CHART	PROCESS TITLE	QC POINT
	Solder-Dipping	
	Q.C Monitor * Temp of S/Bath * Sn in Solder * Solderability	TEMPERATURE. % OF Sn APPEARANCE
	4th Optical Insp.	
	4th O/Gate * Visual	APPEARANCE
	Temp. cycle (Option)	
	Mark & Cure	
	Final Visual/Mech.	
	Initial Class	
	Burn-In (Option)	
	Final Test	
	Q.C Final Gate * Visual	APPEARANCE
	* Electrical	ELECTRICAL PARAMETERS * D.C & SPEED * FUNCTION
	RELIABILITY TEST * LIFE TEST LTPD: 5% * 85/85 TEST LTPD: 10% * PRESSURE POT LTPD: 10% * THERMAL SERIES LTPD: 10% * LEAD INTEGRITY LTPD: 20% * PHYSICAL DIMENSION LTPD: 15%	ENVIRONMENTAL TEST MECHANICAL TEST AND ENDURANCE TEST

FLOW CHART	PROCESS TITLE	QC POINT
	* RESISTANCE TO SOLVENTS LTPD: 15% * SOLDERABILITY LTPD: 10% Packing Q.C Pack Gate Ship * ESD MONITOR (ALL PROCESS)	

3. RELIABILITY TEST

3.1 Principle of Reliability

The fundamental principles of reliability engineering predict that the failure rate of any group of devices as a function of time will follow a curve similar to Figure 1. The curve is divided into three regions: Infant Mortality, Random Failures and Wearout Failures. These regions describe the principal classes of failure mechanisms encountered in that portion of the life of a device.

Infant Mortality represents the early life failures of a device. Failures in this region are usually associated with one or more manufacturing defects. After some period of time the failure rate reaches a low value or the Random failure portion of the curve that represents the useful portion of device life. Infant Mortal failures are eliminated prior to customer shipment by high voltage cell stress, HTRB and reliability screen testing. (Baking Temp Cycle, Burn-IN)

Wearout failures occur at the end of the device's useful life and are characterized by ripidly rising failure rate with time. This does not occur before hundreds of years for integrated circuits.

Associated with each portion of the curve are specific failure mechanisms. These failure mechanisms have been extensively discussed in the literature

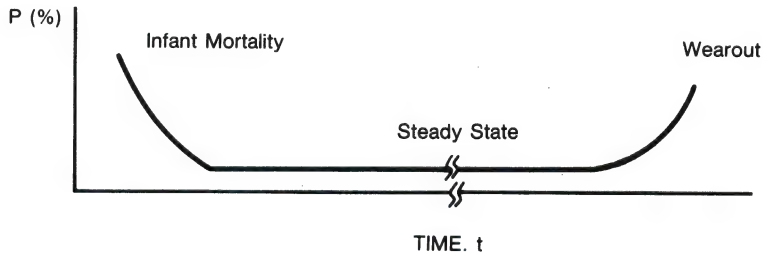


Figure 1. Reliability Life (Bath-tub) Curve

3.2. Reliability Test Items and Conditions

Qualification and quality conformance inspection procedures for all memory devices of the corporation are followed, these procedures assure that the device and lot quality conforms with the requirements of the applicable procedure document. The full requirements of group A. B. C, and D tests and inspectioins are intented for use in change and periodic testing for retention of qualification. Group A and B tests and inspections are performed for quality conformance inspection on individual inspection lots as a condition for acceptance for delivery. Group C and D tests are preformed for quality conformance inspection on a periodic basis as a condition for acception for delivery.

I. Group A: ELECTRICAL TEST

TEST ITEMS	MIL-STD-883C	GOLDSTAR SEMI
1. STATIC TEST (AT 25°C)	LTPD 2: S/S=266 C=2	PPM:400 AQL=0.04% S/S=315 C=0
2. STATIC TEST (AT MAX. OP. TEMP.)	LTPD 3 : S/S=176 C=2	
3. STATIC TEST (AT MIN. OP. TEMP.)	LTDP 5 : S/S=105 C=2	
4. DYNAMIC TEST (AT 25°C)	LTPD 2 : S/S=266 C=2	
5. DYNAMIC TEST (AT MAX. OP. TEMP.)	LTPD 3 : S/S=176 C=2	
6. DYNAMIC TEST (AT MIN. OP. TEMP.)	LTPD 5 : S/S=105 C=2	
7. FUNC. TEST (AT 25°C)	LTPD 2 : S/S=266 C=2	
8. FUNC. TEST (AT MAX. MIN. OP TEMP.)	LTPD 5 : S/S=105 C=2	
9. SWITCHING (AT 25°C)	LTPD 2 : S/S=266 C=2	
10. SWITCHING (AT MAX. OP. TEMP.)	LTPD 3 : S/S=176 C=2	
11. SWITCHING (AT MIN. OP. TEMP.)	LTPD 5 : S/S=105 C=2	

II. Group B: PER LOT

TEST ITEMS	METHOD	MIL-STD-883C	GOLDSTAR SEMI
1. PHYSICAL DIMENSION	2016	n = 2 : c = 0	n = 2 : c = 0
2. RESISTANCE TO SOLVENTS	2015	n = 4 : c = 0	LTPD 15% S/S = 15 C = 0
3. SOLDERABILITY TEST	2022 2003	LTPD 15% S/S = 15 C = 0	LTPD 10% S/S = 22 C = 0
4. INTERNAL VISUAL & MECHANICAL	2014	n = 1 : c = 0	n = 1 : c = 0
5. BOND STRENGTH	2011	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
6. SEAL FINE LEAK GROSS LEAK	1014	LTPD 5% S/S = 45 C = 0	LTPD 5% S/S = 45 C = 0
7. A) ELECTRICAL PARAMETERS B) E.S.D CLASSIFICATION C) ELECTRICAL PARAMETERS	Gr A 3015 Gr A	n = 15 : c = 0	LTPD 10% S/S = 22 C = 0

III. Group C: PERIODIC : DIE-RELATED TESTS

TEST ITEMS	METHOD	MIL-STD-883C	GOLDSTAR SEMI
1. A) STEADY STATE LIFE TEST	1005	AT 125°C : 1000 HRS	AT 125°C:1000 HRS
B) END POINT ELECTRICAL		LTPD 5% S/S = 77 C = 1	LTPD 5% S/S = 77 C = 1
2. A) TEMPERATURE CYCLE	1010	TEST COND. C LTPD 15% S/S = 25 C = 1	TEST COND.C:100 CYCLE LTPD 10% S/S = 38 C = 1
B) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
C) SEAL	1014		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
D) VISUAL EXAMINATION	1011, 1010		
E) END POINT ELECTRICAL			

IV. Group D: PACKAGE RELATED TESTS

TEST ITEMS	METHOD	MIL-STD-883C	GOLDSTAR SEMI
1. PHYSICAL DIMENSION	2016	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
2. A) LEAD INTERGRITY	2004	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
B) SEAL	1014		
FINE LEAK		TEST CON. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
3. A) TEMPERATURE CYCLE	1010	TEST COND.C: 100 CYCLE	TEST COND.C: 250 CYCLE
B) MOISTURE RESISTANCE	1004		
C) SEAL	1004		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
D) VISUAL EXAMINATION	1010 & 1014		
E) END POINT ELECTRICAL			
4. A) MECHANICAL SHOCK	2002	LTPD 15% S/S = 15 COND. B C = 0	LTPD 15% S/S = 15 COND. B C = 0
B) VIBRATION, VARIABLE FREQUENCY	2007	TEST COND. A	TEST COND. A
C) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
D) SEAL	1014		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
E) VISUAL EXAMINATION	1010 & 1011		
F) END POINT ELECTRICAL			
5. ADHESION OF LEAD FINISH	2025	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
6. LID TORQUE	2024	n = 5 : c = 0	n = 5 : c = 0

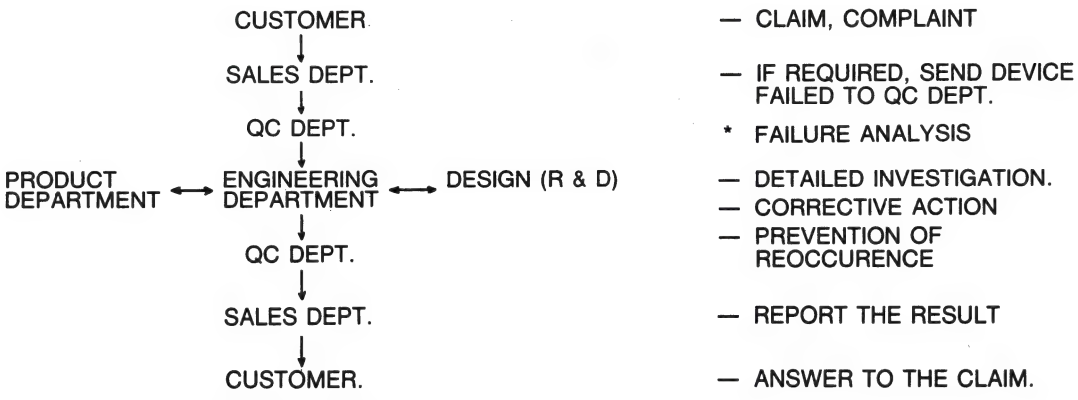
RELIABILITY TEST ITEMS OF GOLDSTAR SEMICONDUCTOR

PLASTIC-DIP ONLY

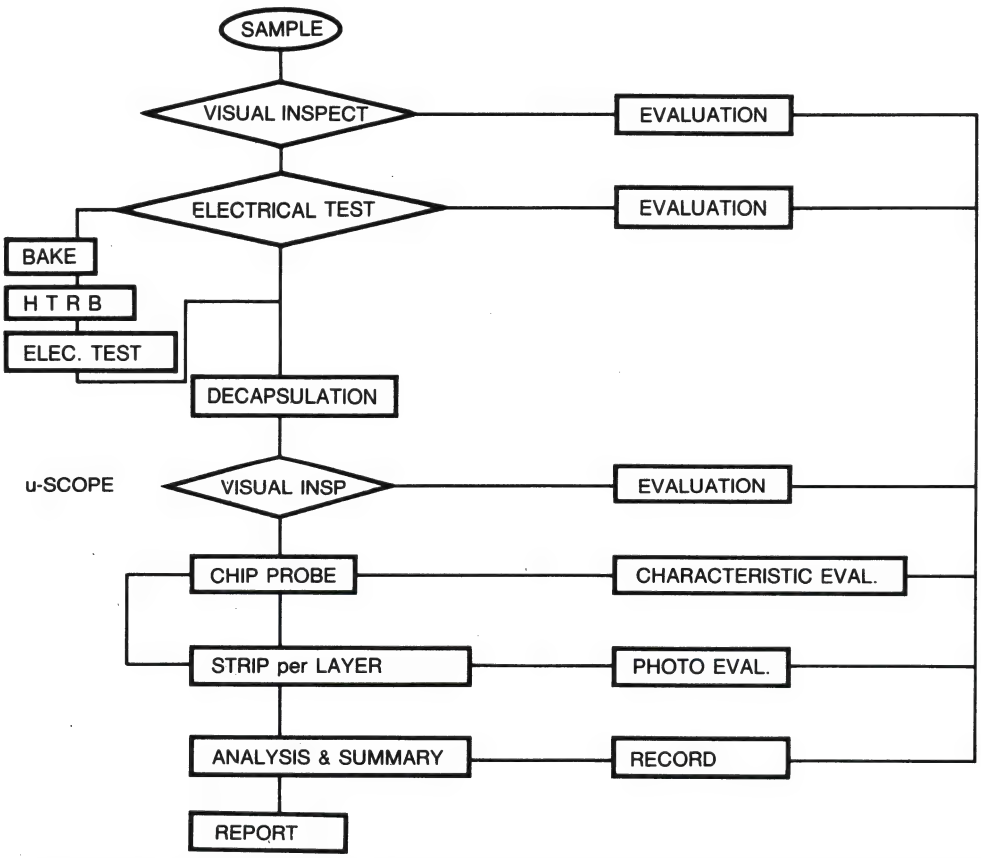
TEST ITEM	TEST CONDITION	QUALITY APPROVAL			QUALITY CONFORMANCE				PURPOSE OF TEST
		S/S	LTPD	#of ACC	TEST	S/S	LTPD	#of ACC	
Visual Inspection	Outgoing Visual Specification	—	—	—	Every Lot		AQL 0.065%	0	scrren out defects
Electrical Test (DC/AC)	Outgoing Test Specification	—	—	—	Every Lot		AQL 0.04%	0	screen out defects
Dimension	Lead Thickness	5	—	0	Every Lot	1	—	0	screen out defects
Dimension	All Dimension	5	—	0	Every Week	1	—	0	screen out defects
Packing Inspection	Outgoing Packaging	—	—	—	Every Lot	All	—	0	screen out defects
High Temperature Operating Life Test	Ta=125C, t=1000 HRS V_{CC}=5V, Dynamic	77	5	1	Every 2 Month	77	5	1	checks resistance to electrical thermal stress applied for long time
High Temperature Storage Test	Ta=150C, t=1000 HRS No Bias	38	10	1	Every 2 Month	38	10	1	checks resitance to heat when exposed to high temperature
Biased Humidity Test	Ta=85C, 85% RH V_{CC}=5V, t=1000	38	10	1	Every 2 Month	38	10	1	checks resistance to long time use with high relative humidity
Pressure Cooker Test	Ta=121C, 30 PSIG 100% RH, 200 HRS	22	15	0	Every 2 Month	22	15	0	checks resistance to accelerated humi-ity changes
Temperature Cycle Test	−65C, 25 C, 150 C 10 Min, 5 Min, 10 Min 250 Cycle	38	10	1	Every 2 Month	38	10	1	checks resistance to high & low temper-atures, and varying temperatures.
Lead Integrity	3X, 90 Arcs, 5 Units	15	15	0	Every 2 Month	15	15	0	checks resistance to forces to which the lead is subject during installation or operation
Solderability	Solder Temp. 240 $\pm$ 5 C Steam Aging 1 HRS Flux 6sec, Solder 5sec	22	10	0	Every 2 Month	22	10	0	checks solerability to leads
Resistance to Solvents		15	15	0	Every Lot	15	15	0	checks resistance of printed marking to solvent
Electro Static Discharge	MIL-STD-883C METHOD 3015	22	10	0	Every Lot	22	10	0	checks resistance to electro static dischange

7. FMA FLOW CHART

PROCEDURE OF FAILURE ANALYSIS



* FAILURE ANALYSIS



4. SUMMARY

This report has presented quality assurance system and reliability test on GoldStar Semiconductor devices. According to the reliability test results and actual experimental data of operating life test, it is concluded that GoldStar devices are high quality devices and the incoming failure rate is expected to be less than 0.04%.

5. HANDLING AND STORAGE INSTRUCTION

5.1 HANDLING PRECAUTIONS

For all devices, the following practices should be observed for protection against high electrical static discharges.

5.1.1 Device leads should be in contact with a conductive material except when being tested or in actual operation.

5.1.2 Conductive parts tools, fixtures, soldering irons and handling equipment should be grounded to handle the devices.

5.1.3 Devices should not be inserted into or removed from test stations unless the power is off.

5.1.4 Neither should signals be applied to the input while the device power supply is in an off condition.

5.1.5 Operators should use grounded wrist straps and work conductive surfaces should be also grounded.

5.2 STORAGING PRECAUTIONS.

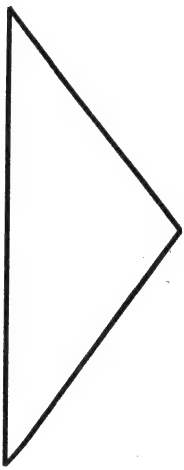
There are several basic requirements in case of long term storage for semiconductor devices.

5.2.1 Store the devices in a covered or sealed antistatic container.

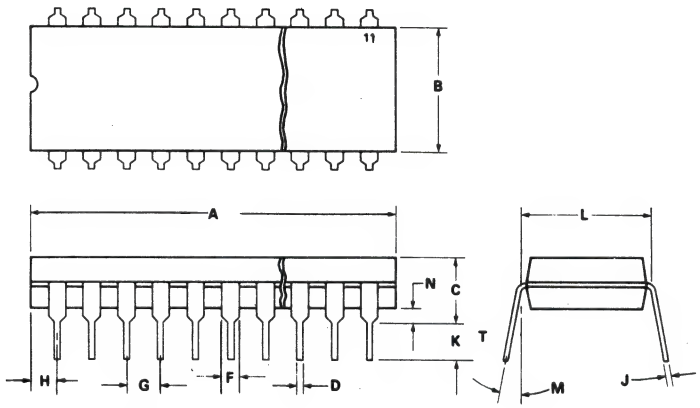
5.2.2 Store the devices in an environment of no more than 60% relative humidity.

5.2.3 Store the devices in a inert atmosphere not exceeding +125°C or no more than −55°C.

5.2.4 Physical force is not permitted on any leads or plastic body when the devices are stored for prevention damage of device.



PLASTIC DIP

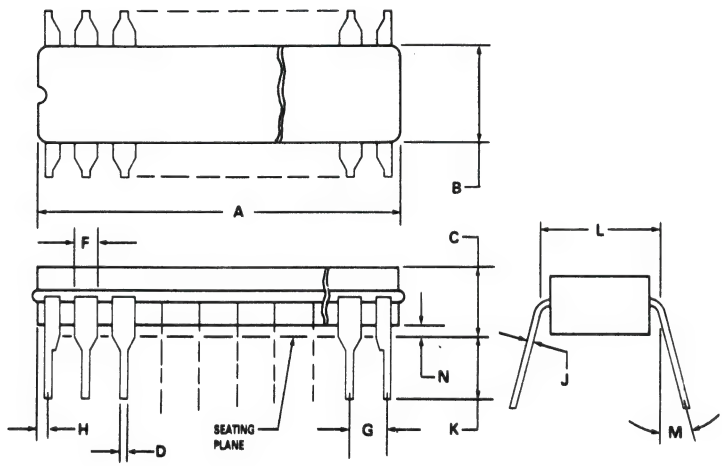


(UNIT: INCHES)

SYMBOL	16 PIN		18 PIN		20 PIN		22 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.738	0.752	0.875	0.900	1.013	1.040	1.095	1.150
B	0.245	0.255	0.245	0.255	0.263	0.273	0.260	0.287
C	0.143	0.152	0.145	0.162	0.143	0.152	0.145	0.160
D	TYP. 0.018		TYP. 0.018		TYP. 0.018		TYP. 0.018	
F	TYP. 0.063		TYP. 0.060		TYP. 0.065		TYP. 0.060	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.015	0.030	0.04	0.05	0.058	0.066	—	0.075
J	0.009	0.014	0.009	0.015	0.009	0.010	0.009	0.010
K	0.125	0.145	0.125	0.130	0.125	0.132	0.125	0.142
L	0.300 BSC		0.300 BSC		0.300 BSC		0.300 BSC	
M	0′	10′	0′	10′	0′	10′	0′	10′
N	0.015	—	0.015	—	0.015	—	0.015	

SYMBOL	24 PIN		28 PIN					
	MIN	MAX	MIN	MAX				
A	1.243	1.260	1.415	1.460				
B	0.535	0.545	0.535	0.545				
C	0.158	0.170	0.158	0.170				
D	TYP. 0.018		TYP. 0.018					
F	TYP. 0.060		TYP. 0.060					
G	0.09	0.11	0.09	0.11				
H	0.06	0.075	0.06	0.076				
J	0.009	0.015	0.009	0.015				
K	0.125	0.132	0.125	0.132				
L	0.600	0.625	0.600	0.620				
M	0′	10′	0′	10′				
N	0.008	—	0.008	—				

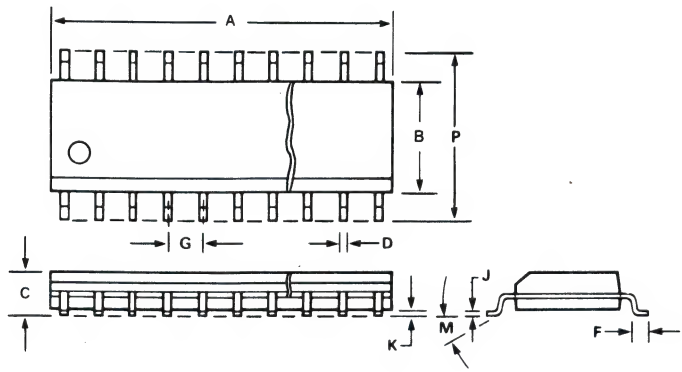
CER DIP



(UNIT : INCHES)

SYMBOL	16 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.753	0.785	0.940	0.985	1.240	1.290	1.440	1.485
B	0.272	0.294	0.265	0.306	0.514	0.526	0.514	0.598
C	0.165	0.200	0.165	0.200	0.165	0.200		0.225
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.023
F	0.055	0.065	0.055	0.065	0.055	0.065	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.012	0.060	0.012	0.060	0.040	0.098	0.040	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.590	0.620	0.590	0.620
M	0′	10′	0′	10′	0′	10′	0′	10′
N	0.02	0.06	0.02	0.07	0.02	0.07	0.02	0.07

SOP

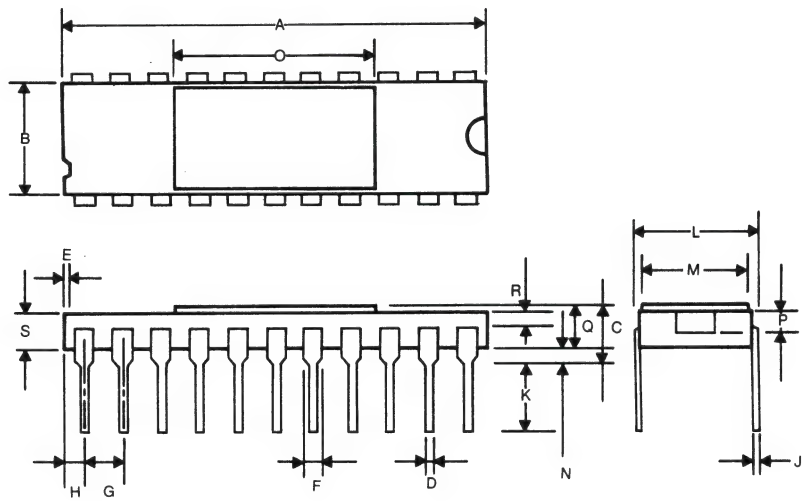


(UNIT : INCHES)

CODE NO.	20 F		24 F		24 FW			
PIN	20 PIN		24 PIN		24 PIN			
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX		
A	0.496	0.510	0.602	0.614	0.622	0.638		
B	0.292	0.299	0.292	0.299	TYP. 0.331			
C	0.097	0.104	0.097	0.104	—	0.098		
D	0.014	0.019	0.014	0.019	0.012	0.018		
F	0.018	0.035	0.018	0.035	TYP 0.039			
G	0.050 BSC		0.050 BSC		0.050 BSC			
J	0.010 BSC		0.010 BSC		0.010 BSC			
K	0.004	0.008	0.0055	0.0115	0.004			
P	0.400	0.410	0.400	0.410	0.453	0.477		
M	0′	8′	0′	8′	—	—		

CODE NO.	28 F		28 FW					
PIN	28 PIN		28 PIN					
SYMBOL	MIN	MAX	MIN	MAX				
A	0.703	0.712	0.720	0.750				
B	0.292	0.289	TYP. 0.331					
C	0.097	0.104		0.098				
D	0.014	0.019	0.012	0.018				
F	0.018	0.035	TYP. 0.039					
G	0.050 BSC		0.050 BSC					
J	0.010 BSC		0.010 BSC					
K	0.0055	0.0115	0.004	—				
P	0.400	0.410	0.453	0.477				
M	0′	8′	—	—				

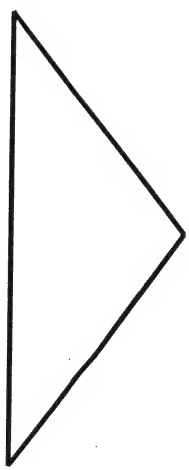
SIDE BRAZED



(UNIT: INCHES)

SYMBOL	22 PIN	
	MIN	MAX
A	1.088	1.112
B	0.281	0.298
C	—	0.160
D	0.016	0.020
E	0.004	—
F	TYP. 0.050	
G	0.09	0.105
H	0.035	0.065
J	0.009	0.011

SYMBOL	22 PIN	
	MIN	MAX
K	0.14	0.170
L	0.290	0.310
M	0.265	0.275
N	0.020	0.050
O	0.555	0.565
P	TYP. 0.050	
Q	0.092	0.122
R	0.005	—
S	0.08	—



GOLDSTAR SEMICONDUCTOR SALES NETWORK

ASIA

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° KUM SUNG JUN SIN ELECTRONICS CO,. LTD.
182-13, Jangsa-Dong, Chongro-Gu
Seoul, Korea
Tel:02-273-6811/3,274-1911/2
Fax:02-272-4367

° SAM JIN ELECTRONICS
671-1, Junpo 1 Dong Busanjingu
Busan, Korea
Tel:051-807-1717 / 1747
Fax:051-807-6657

° SEOG YUNG ELECTRONICS
182-2, Jangsa-Dong, Chongro-Gu
Seoul, Korea
Tel:02-273-6781
Fax:02-273-6597

° SOKCHUN TRADING CO.,LTD.
3112 Sun-In B/D Young San
K.P.O.Box 1148, Seoul, Korea
Tel:02-273-7877/3177, 266-1940
701-7811/7814
Fax:02-274-3291

° WOO SUNG SEMICONDUCTOR
5005Ho 22Dong Seonin Sangga
16-1, Hangangro-2Ga, YongSan-Gu
Seoul, Korea
Tel:02-273-4730, 272-3874
701-0291-4
Fax:02-701-0295

HONG KONG

* GOLDSTAR (H.K.) LTD.
Rm. 1501B, World Wide House,
19, Des Voeux Road, Central,
Hong Kong.
Tel:5-845-6787
Fax:5-845-9416

* LUCKY-GOLDSTAR INT'L LTD.
Rm. 3001, Gloucester Tower
30th Fl. The Landmark
Central, Hong Kong
Tel:5-26-6402/7
Fax:5-868-1460

•DYNATEK ELECTRONICS LTD.
Unit 701, 7/F., Hong Leong Industrial Complex,
4 Wang Kwong Road, Kowloon Bay, Hong Kong
Tex:3-796-6689
Fax:3-796-6109

•SUN COMPONENTS LTD.
1/F Hang Lung Bank Bldg.
46-48 Granville Road
TsimShaTsui, Kowloon, H.K.
Tel:3-311-8321
Fax:3-311-6715

•TECHGROW LTD.
4B Cheerful Comm. Bldg.
116-118, Ma Tau Wai Rd. Hunghom,
Kowloon
Hong Kong
Tel:3-764-3618
Fax:3-764-1781

INDIA

* GOLDSTAR CO., LTD.
Room 306-309 Parkash Deep Bldg.
7, Tolstoy Marg.
New Delhi 110 001, India
Tel:11-331-1899
Fax:11-332-3754

* LUCKY-GOLDSTAR INT'L CORP.
Room 306-309 Parkash Deep Bldg.
7, Tolstoy Marg.
New Delhi 110 001, India
Tel:11-331-1899
Fax:11-332-3754

•SEMICON TECH
15, Amrut Hansoti Rd.
Cama lane, Ghatkopar (W)
Bombay 400 086, India
Tel:22-511-4789
Fax:22-513-6940

•SPARTEX SYSTEMS & SERVICES PVT. LTD.
No. 68, Michael Palyam,
Near Deccan Studio, C.V. Raman Nagar Post
Bangalore 560 093, India
Tel:812-56-4211
Tlx:8452190 MLHR IN

JAPAN

* GOLDSTAR JAPAN CO., LTD.
Hon-Kan 9F. Akasaka Twin Tower
17-22, 2-Chome, Akasaka, Minato-ku
Tokyo, Japan
Tel:03-224-0123
Fax:03-582-7948

•JAPAN MACNICS CORP.
516, Imaiminami-Cho, Nakahara-Ku
Kawasaki-City, Kanagawa-Ken, 211
Japan
Tel:044-711-0022
Fax:044-711-2214

•OHTORI CORP.
9-8, 5 Chome,
Nipponbashi, Naniwa-Ku,
Osaka Japan
Tel:06-643-1655
Fax:06-633-5212

•OKAMOTO MUSEN CO., LTD. TOKYO BRANCH
3-2-17 Nozawa, Setagaya-Ku
Tokyo 154, Japan
Tel:03-412-8211
Fax:03-418-2555

SINGAPORE

* GOLDSTAR CO., LTD.
8 Shenton Way
#30-04 Treasury Bldg.
S'pore 0106
Tel:224-3166
Fax:224-0721

* LUCKY-GOLDSTAR INT'L CORP.
8 Shenton Way
#39-03 Treasury Bldg.
S'pore 0106
Tel:220-4566
Fax:224-9049

•DYNAMAR HOLDINGS PTE LTD.
109 Defu Lane 10
Singapore 1953
S'pore 1334
Tel:281-3388
Fax:281-3308

TAIWAN

* GOLDSTAR CO., LTD. TAIPEI OFFICE
12F-3, No. 148, Chung-Hsiao
E.Rd. SEC. 4 Taipei, Taiwan, R.O.C.
Tel:02-731-6528/9
Fax:02-731-6530

* LUCKY-GOLDSTAR INT'L CORP.
3F-4, NO. 695
Tun Hwa South Road, Taipei,
Taiwan, R.O.C.
Tel:02-755-6648/6650
Fax:02-702-0687

•BRIGHT UP INDUSTRIES CO., LTD.
12F, N0. 142, Chung-Hsiao
E. Rd. SEC. 4 Taipei, Taiwan, R.O.C.
Tel:02-773-2194/8, 776-5455/9
Fax:02-751-9545

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Tel:02-507-1186
Fax:02-508-2250

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14th Fl., 687 Ming Sheng East Rd. Taipei, Taiwan, R.O.C.
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Tel:02-776-0560/5
Fax:02-731-3100

EUROPE

AUSTRIA

* LUCKY-GOLDSTAR INT'L CORP.
Mariahilfer Strasses 77-79, 1060, Wien, Austria
Tel:222-93-3747
Fax:222-93-3739

° E.S.L. HANDELSGES M.B.H.
Wasagasse 26/3B
A-1090,Wien, Austria
Tel:222-310-1025
Fax:222-310-1027

BELGIUM

° MALCHUS ELECTRONICS
Plantin-moretuslei 172
B-2018 Antwerpen, Belgium
Tel:3-235 32 72
Fax:3-271 10 49

DENMARK

° OLE WOLFF ELEKTRONIK APS.
Rodengvej 25, Dk 4180 Soro. Denmark
Tel:3-63-3830
Fax:3-63-0183

FINLAND

° ELDIS OY
Niittyrinne 6, 02270, Espoo, Finland
Tel:0-803-9044
Fax:0-803-9089

FRANCE

* LUCKY-GOLDSTAR INT'L CORP.
PARIS OFFICE
24, Avenue De La Grande-Armee
75017 Paris, France
Tel:1-47 66 88 88
Fax:1-47 66 13 80

¤ AGEREP
7, rue Marcelin Berthelot
92160 ANTONY, France
Tel:1-46 66 60 33
Fax:1-40 96 92 26

° COMPTOIR COMMERCIAL D'IMPORTATION
5, rue Marcelin Berthelot
92160 Antony, France
Tel:1-46 66 21 82
Fax:1-40 96 92 26

° ERICSSON COMPOSANTS
B.P. 203, 78051 Saint-Quentin Yvelines Cedex, France
Tel:1-30 58 24 24
Fax:1-30 58 30 96

ITALY

° DAEWON EUROPA S.R.L.
Via lenardo da vinci, 43
20090 Trezzano Sul Naviglio (Milano), Italy
Tel:2-44 50 042
Fax:2-44 50 184

° MELCHIONI S.P.A.
Via P. Colletta,37
20135 Milano, Italy
Tel:2-57 941
Fax:2-5 51 81 914

NETHERLANDS

° MALCHUS B.V.
P.O. Box 4S
3100AA Schiedem, Netherlands
Tel:10-427 77 77
Fax:10-415 48 67

NORWAY

° FEIRING ELEKTRONIKK A/S
P.O. Box 101, Bryn,
0611 Oslo 6, Norway
Tel:2-64 9070
Fax:2-64 4051

SPAIN

° INDUTRONIK,S.A.
Angelita Cavero,9
28027 Madrid, Spain
Tel:1-741 80 11
Fax:1-742 68 31

° LOBER, S,A.
Monte Esquinza, 28
E-28010 Madrid, Spain
Tel:1-410 68 21
Fax:1-410 69 68

SWEDEN

° MIKO KOMPONENT AB
Seger Sbyvagen 3
S-14502 Norsborg, Sweden
Tel:753-890 80
Fax:753-753 40

SWITZERLAND

° ETRONICS AG
Sonnenberg, P.O.B.23
8103 Unterengstringen, Switzerland
Tel:1-750 35 11
Fax:1-750 35 67

TURKEY

° COMTEC San. ve Tic. Koll. Sti.
Hasanpasa, Ahmet Rasim Sok,
No. 16 Kadikoy Istanbul, Turkey
Tel:1-337-2245
Tlx:29569 ELTS TR
Fax:1-336-8814

U.K.

* GOLDSTAR CO., LTD.
Goldstar House 264 Bath Road Slough Berkshire Sli 4EW
Tel:753-69-1888
Fax:753-69-3061

* : Sales Offices
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GOLDSTAR SEMICONDUCTOR SALES NETWORK

* LUCKY-GOLDSTAR INT'L LTD.
1-Fl, Califton House 83-89
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London W5 5TA, U.K.
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Industrial Estate ST Ives, Cambridge
Shire PE17 4WJ
Tel:0480-49-6466
Fax:0480-49-6621

W. GERMANY

* GOLDSTAR Deutschland GmbH
Zentrale Ratingen
HarkortstraBe 41
D-4030 Ratingen
Tel:02-102-4987-0
Fax:02-102-4996-62

* LUCKY-GOLDSTAR INT'L (Deutschland) GmbH
Lyoner Stern Bldg.
Hahnstrasse 70
D-6000 Frankfurt Am Main 71
W.Germany
Tel:69-663-0070
Fax:69-666-6865

° BECK GmbH & CO. ELEKTRONIK
Bnauelemente KG. Postfach
91,02 80 8500 Nuernberg 91, W.Germany
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Tlx:622334 BECK D
Fax:0911-340-528

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P.O. Box 610 H.W.
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Tlx:20348 MOMA

NORTH AMERICA

U.S.A.

* GOLDSTAR TECHNOLOGY, INC.
3003 North First Street,
San Jose, CA 95134-2004
Tel:408-432-1331
Fax:408-432-6053

* GOLDSTAR TECHNOLOGY, INC. EASTERN AREA OFFICE
8410 W.Bryn Mawr Avenue Suite
900 Chicago, IL 60631-3430 U.S.A.
Tel:312-693-0450
Fax:312-399-0817

* GOLDSTAR TECHNOLOGY, INC. WESTERN AREA OFFICE
6576 Corte Cisco
Calsbad. CA 92008
Tel:619-931-7641
Fax:619-931-9628

ALABAMA

¤ EMA
WESTERN REGIONAL OFFICE
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Tel:619-565-1944
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3333 Bowers. Suite 251
Santa Clara, CA 95054
Tel:408-727-8753
Fax:408-727-8573

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31887 Circle Drive
Laguna Beach, CA92677
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Fax:714-499-1580

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San Jose, CA 95131
Tel:408-943-1200
800-222-6001
Fax:408-943-1393

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Fax:408-432-9298

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Santa Clara, CA 95050
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Fax:408-986-9584

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Torrance, CA 90501
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800-669-8300
Fax:213-320-7207

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1582 Parkway Loop, Unit G
Tustin. CA 92680
Tel:714-259-8258
Fax:714-259-0828

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3320 East Mineral King, Unit D
Visalia, CA 93291
Tel:209-734-8861
Fax:209-734-8865

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Fax:818-889-2472

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Tel:407-339-3855
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Boca Raton, FL 33431
Tel:407-368-7373
Fax:407-394-5441

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1417 Malabar Lakes Drive N.E.
Palm Bay, FL 32905
Tel:407-984-0669
Fax:407-951-0906

¤ LAWRENCE ASSOCIATES, INC.
1131 US 19 South
Palm Harbor, FL 34864
Tel:813-787-2773
Fax:813-787-2654

° ALL AMERICAN SEMICONDUCTOR, INC.
16251 N.W. 54th Avenue
Miami. FL 33014
Tel:305-621-8282
Fax:305-620-7831

° ALL AMERICAN SEMICONDUCTOR, INC.
5009 Hiatus Road
Sunrise, FL 33351
Tel:305-572-7999
Inside FL: 800-432-6838
Outside FL: 800-327-6237
Fax:305-749-9229

° JACO ELECTRONICS, INC.
1202 Tech. Blvd., Suite 201
Tampa. FL 33619
Tel:813-628-4665
Toll Free from N.FL & GA:800-265-JACO
Fax:813-626-8185

GEORGIA

¤ EMA
EASTERN REGIONAL OFFICE
620 Colonial Park Drive
Roswell, GA 30075
Tel:404-992-7240
Fax:404-993-3426

ILLINOIS

¤ SYNERGISTICS SALES INC.
501 Mitchel Road
Glendale Heights, IL 60139
Tel:312-858-8186
Fax:312-790-9799

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7110-16N. Lyndon Street
Rosemont, IL 60018
Tel:312-298-4210
Fax:312-297-6650

° Q.P.S. ELECTRONICS, INC.
101 East Commerce Dr.
Schaumberg, IL 60173
Tel:312-884-6620

INDIANA

° ADVENT ELECTRONICS, INC.
8446 Molier Road
Indianapolis, IN 46268
Tel:317-872-4910
Fax:317-872-9987

IOWA

° ADVENT ELECTRONICS, INC.
682 58th Ave. Ct. S.W.
Cedar Rapids, IA 52404
Tel:319-363-0221
Fax:319-363-4514

MARYLAND

° JACO ELECTRONICS, INC.
10270 Old Columbia Road
Columbia. MD 21046
Tel:301-995-6620
Fax:301-995-6032

° ALL AMERICAN SEMICONDUCTOR, INC.
14636 Rothger Drive
Rockville, MD 20850
Tel:301-251-1205
800-426-0420
Fax:301-251-8574

MASSACHUSETTS

¤ ALPHA OMEGA SALES CORP.
325 Main Street. Suite 301
North Reading, MA 01864
Tel:508-664-1118
Fax:508-664-3212

¤ ALPHA OMEGA SALES CORP.
10-G Roessler Road
Woburn, MA 01801
Tel:617-933-0237
Fax:617-938-8416

° ALL AMERICAN SEMICONDUCTOR, INC.
107 Audubon Rd., Suite 104
Wakefield, MA 01880
Tel:617-246-2300
800-874-2834
Fax:617-246-2305

MICHIGAN

° ADVENT ELECTRONICS, INC.
24713 Crestview Ct.
Farmington Hills, MI 48331
Tel:313-477-1650
Fax:313-477-2830

MINNESOTA

¤ COMPONENTS GROUP CORP.
45 Groveland Terrace
P.O/Box 3978
Minneapolis, MN 55403
Tel:612-374-1250
Fax:612-374-5434

* : Sales Offices
¤ : Sales Representatives
° : Sales Distributors
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GOLDSTAR SEMICONDUCTOR SALES NETWORK

° ALL AMERICAN SEMICONDUCTOR, INC.
8053 E. Bloomington Fwy., #102
Minneapolis, MN 55420
Tel:612-884-2220
Inside MN:800-223-7364
Outside MN:800-342-7364

NEW YORK

¤ ERA
364 Veterans Memorial Hwy.
Commack, NY 11725
Tel:516-543-0510
Fax:516-543-0758

° JACO ELECTRONICS, INC.
145 Oser Avenue
Hauppauge, NY 11788
Tel:516-273-5500
Fax:516-273-5528

° ALL AMERICAN SEMICONDUCTOR, INC.
711-2 Koehler Avenue
Ronkonkoma, NY 11779
Tel:516-981-3935
Inside NY:800-637-7769
Outside NY:800-874-2830
Fax:516-981-3947

NORTH CAROLINA

¤ EMA
RALEIGH OFFICE
6604 Six Forks Road
Suite 204
Raleigh, NC 27609
Tel:919-846-6888
Fax:919-847-7360

OHIO

¤ K. W. ELECTRONICS, INC.
HEAD OFFICE
8514 N. Main Street
Dayton, OH 45415
Tel:513-890-2150
Fax:513-890-5408

¤ K. W. ELECTRONICS, INC.
BRANCH OFFICE
3645 Warrensville Center #244
Shaker Heights, OH 44122
Tel:216-491-9177
Fax:216-491-9102

° CAM RPC
749 Miner Road
Highland Hts., OH 44143
Tel:216-461-4700
Fax:216-461-4329

OKLAHOMA

¤ LOGIC ONE
6550 East 71St. Suite B
Tulsa, OK 74133
Tel:918-494-0765

PENNSYLVANIA

¤ CMS MARKETING
715 Twining Road
Dresher, PA 19025
Tel:215-885-4424
Fax:215-885-3736

° CAM RPC ELECTRONICS
620 Alpha Drive
Pittsburgh, PA 15238
Tel:412-782-3770
Fax:412-963-6210

TEXAS

¤ LOGIC ONE
11149 Research Blvd. Suite 110
Austin, TX 78759
Tel:512-345-2952
Fax:512-346-5309

¤ LOGIC ONE
4606 FM 1960 West Suite 418
Houston, TX 77069
Tel:713-444-7594
Fax:713-444-8236

¤ LOGIC ONE
200 East Spring Valley Suite AA
Richardson, TX 75081
Tel:214-234-0765
Fax:214-669-3042

° A.V.E.D.
SOUTHWEST, INC.
6448 Hwy 290 East. #A103
Austin, TX 78723
Tel:512-454-8845
Fax:512-459-8043

° A.V.E.D.
SOUTHWEST, INC.
4470 Spring Valley Road
Dallas. TX 75244
Tel:214-404-1144
Fax:214-404-1194

° ALL AMERICAN SEMICONDUCTOR, INC.
1819 Firman Drive. #127
Richardson, TX 75081
Tel:214-231-5300
800-541-1435
Fax:214-437-0353

UTAH

° A.V.E.D.
ROCKY MOUNTAIN, INC.
1836 Parkway Blvd.
West Valley City, UT 84119
Tel:801-975-9500
Fax:801-977-0245

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¤ MICRO SALES, INC.
2122-112th AVE., N.E
Bellevue, WA 95054
Tel:206-451-0568
Fax:206-453-0092

° JACO ELECTRONICS, INC.
15014 N.E. 40th St.
Bldg. "0" Unit 202
Redmond, WA 98052
Tel:206-881-9200
Fax:206-881 9777

CANADA

BRITISH COLUMBIA

¤ VITEL ELECTRONICS
CALGARY OFFICE
4211 Kingsway, Suite #314
Burnaby, British Columbia
V5H 126
Tel:604-439-1136
Fax:604-439-0195

ONTARIO

¤ VITEL ELECTRONICS
OTTAWA OFFICE
300 March Rd., Suite #301
Kanata, Ontario K2K 2E3
Tel:613-592-0090
Fax:613-592-0182

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¤ : Sales Representatives
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● : Sales Representatives/Distributors

GOLDSTAR SEMICONDUCTOR SALES NETWORK

¤ VITEL ELECTRONICS
TORONTO OFFICE
5925 Airport Rd., Suite #610
Mississauga, Ontario LAV 1W1
Tel:416-676-9720
Fax:416-676-0055

° SEMI SPECIALISTS OF CANADA
5080 Timberlea Blvd. #4
Mississauga Ontario, Canada Lawaml
Tel:416-629-9494
Fax:416-629-9493

QUEBEC

¤ VITEL ELECTRONICS
HEAD OFFICE -
MONTREAL
2235 Omesime Gagnon
Lachine, Quebec H8T 927
Tel:514-636-5951
Fax:514-636-5526

° ZANIN ELECTRONIQUE INC.
136 Merizzi, ST-Laurent Quebec,
Canada HAT 154
Tel:514-342-6211
Fax:514-342-4073

SOUTH AMERICA

BRAZIL

* LUCKY - GOLDSTAR INT'L BRAZIL S/C LTDA.
Avenida Paulista, 1.439 -13.
CONJ.134 -CEP 01311 Sao Paul,
Brazil
Tel:11-284-1184/287-4118
Fax:11-285-1997

• UNITY COM. IMP. EXP. LTDA.
Rua Estela, 515 Bloco A - CJ. 142
04011 S.Paulo, Brazil
Tel:11-549-0799/572-5191
Fax:11-572-5191

MEXICO

° DICOPEL
Tochtli 368 Fracc. Ind.
Sn. Antonio, Azcapotzalco
C.P. 02760 Mexico, D.F.
Tel:561-32-11
Fax:561-12-79

* : Sales Offices
¤ : Sales Representatives
° : Sales Distributors
• : Sales Representatives/Distributors

인간과 기술의 만남

Technopia

GoldStar

GOLDSTAR ELECTRON CO., LTD.
HEAD OFFICE : #50. Hyangjeong-Dong,
Cheongju, Chungcheongbuk-Do
SEOUL OFFICE (SALES) #20. Yoido-Dong,
Yeongdeungpo-Gu, Seoul 150-010, Korea
Tel : International (02) 787-3811 ~ 3819
Domestic (02) 787-3801 ~ 3807
Fax : (02) 785 - 7770
Tlx : GSRADIO K23751 SEOUL

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